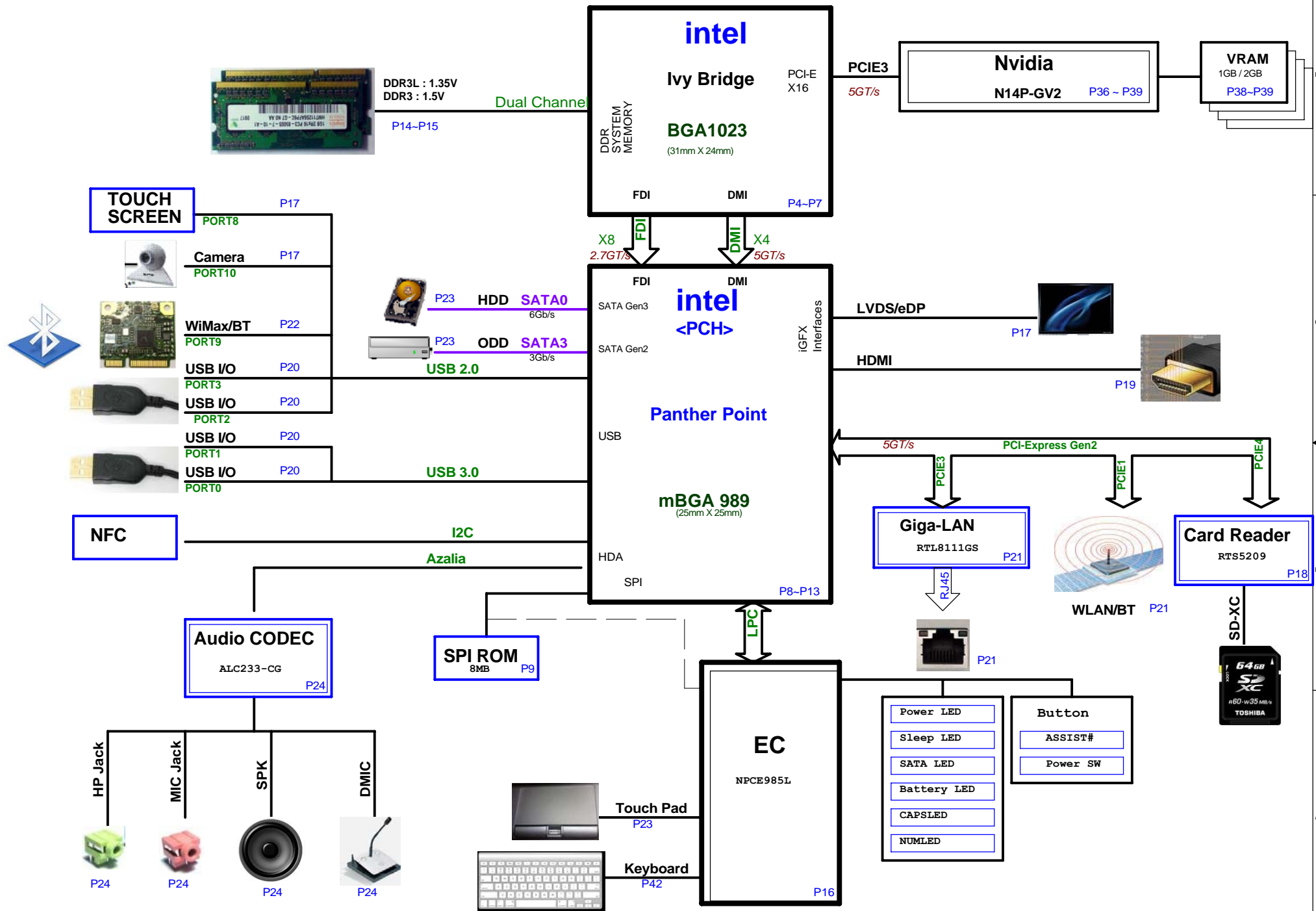


Page	Title of schematic page	Rev.	Date	Page	Title of schematic page	Rev.	Date
01	Page List	1A		42	HOLE/EMI/KB	1A	
02	Block Diagram	1A		43	AUDIO Woofer	1A	
03	Change List	1A		44	IO PORT LIST	1A	
04	IVY 1/4 (HOST&PCIE)	1A				1A	
05	IVY 2/4 (DDR3 I/F)	1A		<div>* : No mount</div> <div>L@ : For LVDS output</div> <div>D@ : For eDP output</div> <div>E@ : For DIS GFX</div> <div>I@ : For UMA</div>			
06	IVY 3/4 (POWER)	1A					
07	IVY 4/4 (GND/Strap)	1A					
08	PCH 1/6 (DMI/FDI/VIDEO)	1A					
09	PCH 2/6 (SATA/RTC/HDA/LPC)	1A					
10	PCH 3/6 (PCIE/USB/CLK/NV)	1A					
11	PCH 4/6 (GPIO/CPU/STRAP)	1A					
12	PCH 5/6 (POWER)	1A					
13	PCH 6/6 (GND)	1A					
14	DDR3 DIMM-0-STD	1A					
15	DDR3 DIMM-1-STD	1A					
16	WPCE985L & FLASH	1A					
17	LVDS/CAMERA	1A					
18	CARD READER (RTS5209)	1A					
19	HDMI/THERMAL	1A					
20	USB	1A					
21	LAN (RTL8111GS)	1A					
22	WLAN/KB-BL	1A					
23	HDD/ODD/G-SENSOR/TP/FAN	1A					
24	Audio ALC233-CG	1A					
25	LED/PS/DMIC	1A					
26	POWER +VCC_CORE (ISL95835)	1A					
27	POWER 3VPCU&RVCC5 (PM6686)	1A					
28	POWER 1.5VSUS/VTT_MEM	1A					
29	POWER +1.05V (G5602R41U) -15A	1A					
30	POWER VCCSA/VCCIO	1A					
31	POWER VCC1.8/Thermal	1A					
32	POWER (BAT IN / ADA IN/ UL)	1A					
33	POWER CHARGER (ISL88731C)	1A					
34	POWER VGA_CORE ( RT8812A)	1A					
35	POWER VCC1.5_VRAM/1.05V	1A					
36	NVIDIA N14 GB2-64 PCIE 1/4	1A					
37	NVIDIA N14 GB2-64 TMDS 2/4	1A					
38	NVIDIA N14 GB2-64 VRAM 3/4	1A					
39	NVIDIA N14 GB2-64 VRAM 4/4	1A					

# Chief River ULV BLOCK DIAGRAM

02

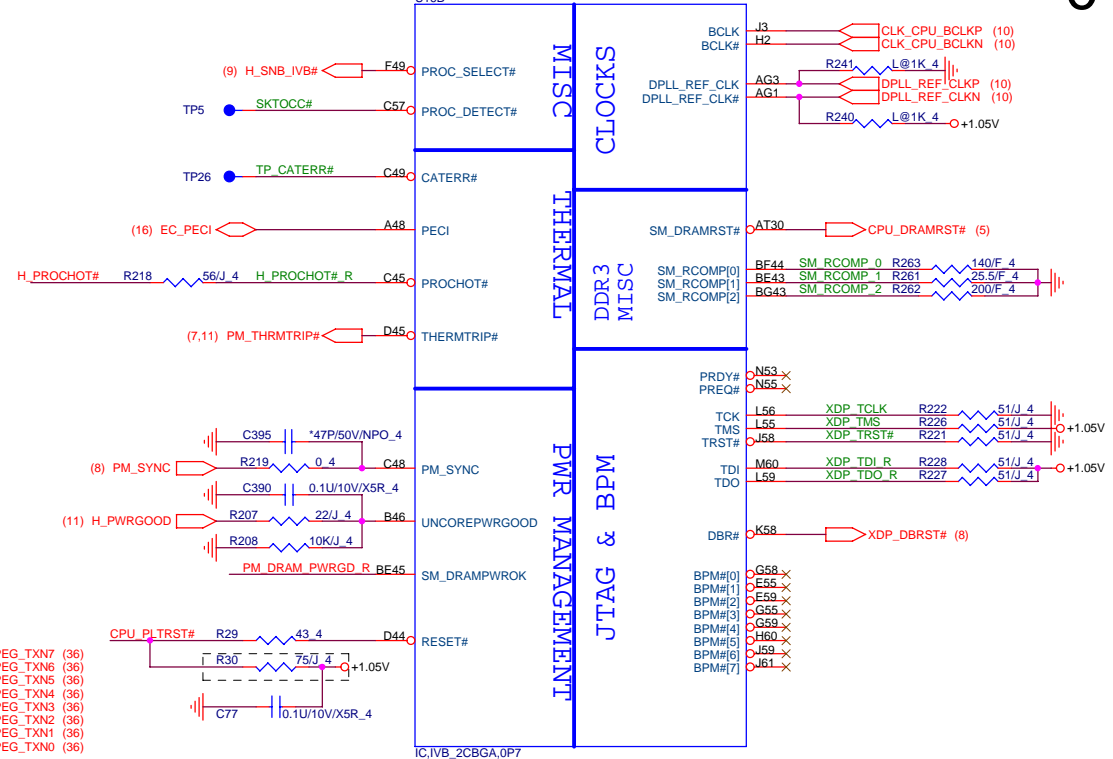
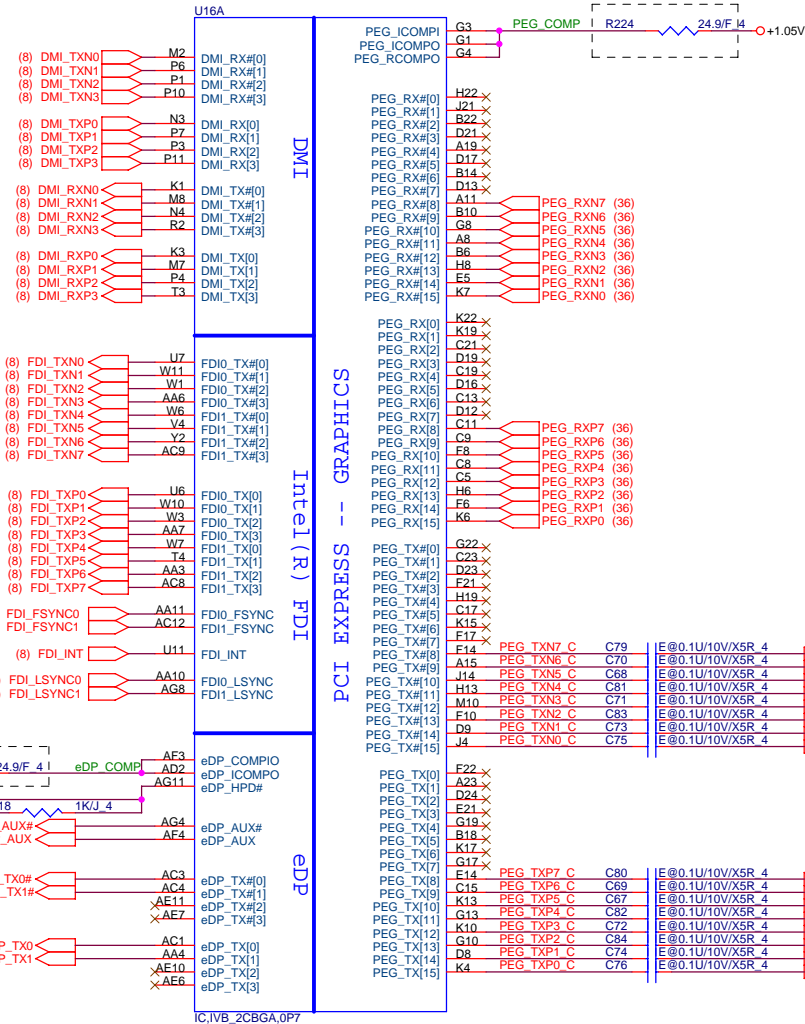


**Change List**  
**MB\_SCH\_PVT\_001**  
P22-Add R333 0\_6S.  
P22- U15 don't mount  
P22-Add Q32(2N7002).  
P22-Add R335(100K\_4).  
  
Reason : Modify circuit for KB Backlight.  
Possible Risk: No.  
**MB\_SCH\_PVT\_002**  
P23-CON11.11 delete net"DATA\_ODD\_DA#  
P10-U17.G40 delete net"SATA\_ODD\_DA#".  
P10-Delete R64(10K\_4).  
  
Reason : Modify circuit for Zero Power ODD.  
Possible Risk: No.  
**MB\_SCH\_PVT\_002**  
P08-ADD 0.1UF on "PCH\_PWROK\_EC"  
  
Reason : Modify circuit for ESD.  
Possible Risk: No.

# Ivy Bridge Processor (DMI,PEG,FDI)

# Ivy Bridge Processor (CLK,MISC,JTAG)

04



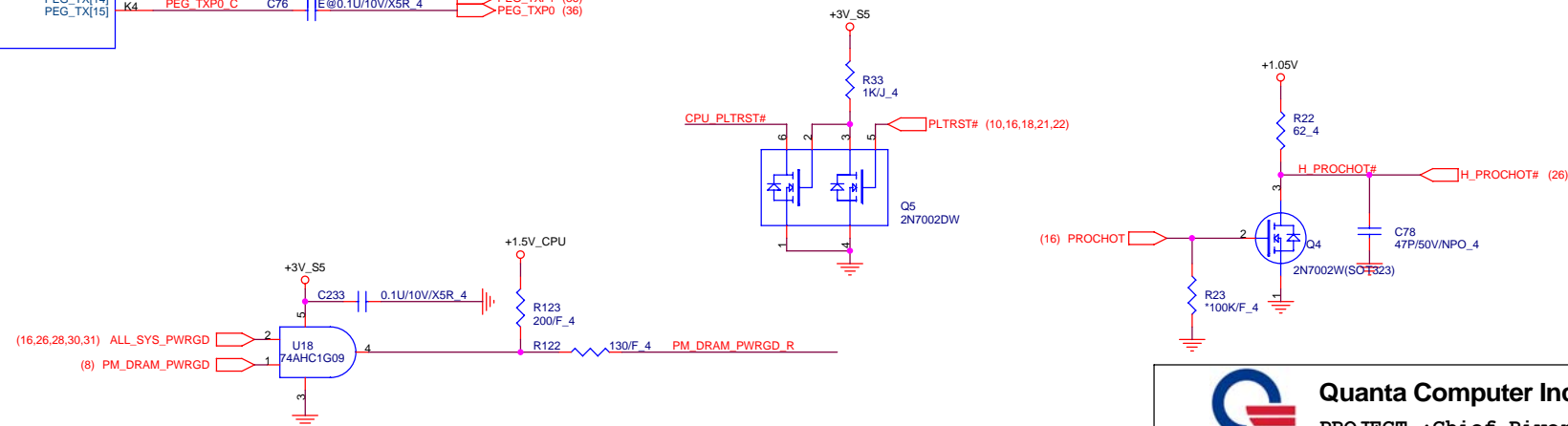
SNB\_IVB#:

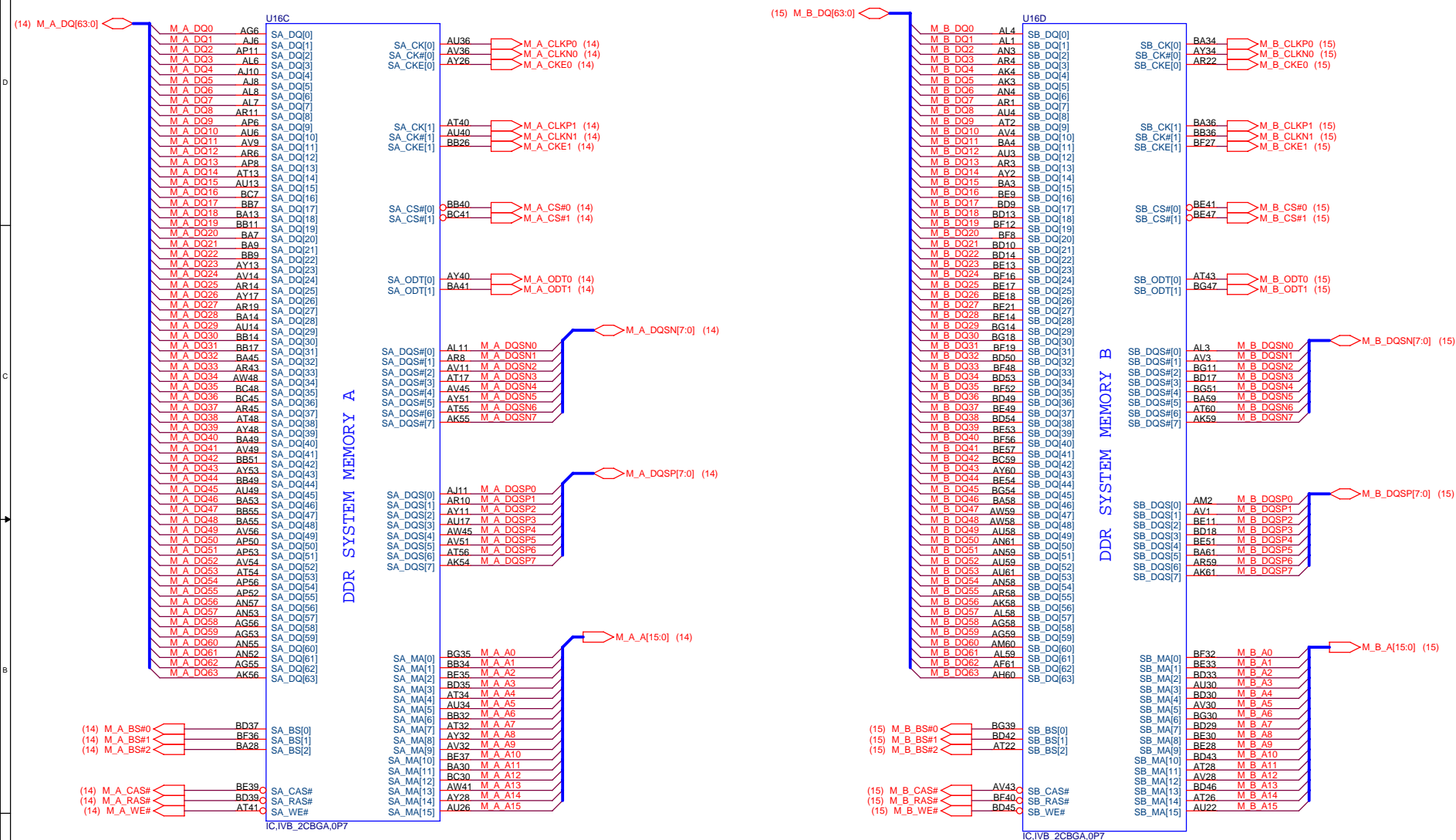
- It is NC when using Sandy Bridge.(1.05V)
- For next generation processor it will be grounded.(1.0V)

**FDI Disabling (Discrete Only)**

FDI\_FSYNC (J18/J17/J19/H17) can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

FDI\_INT connect to GND with 1K ohm.





Quanta Computer Inc.

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Size Document Number  
SNB/IVB 2/4

Rev  
1A

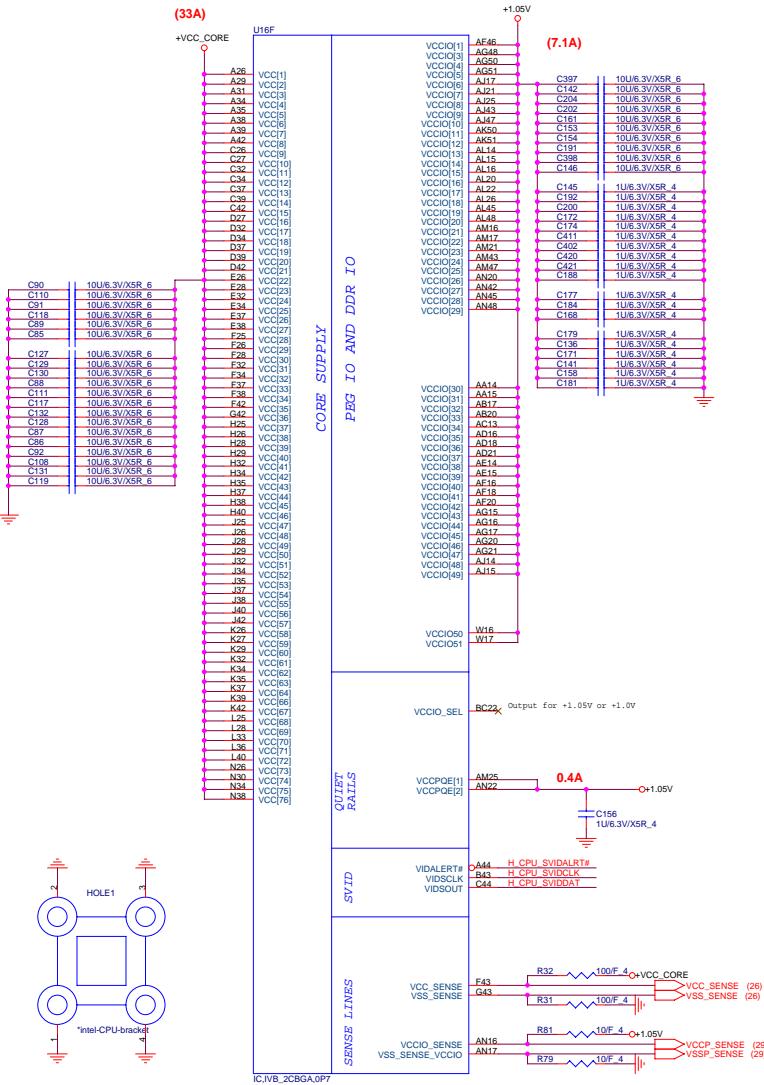
1.Level 1 Environment-related Substances Should Never be Used.

2.Recycled Resin and Coated Wire should be procured from Green Partners.

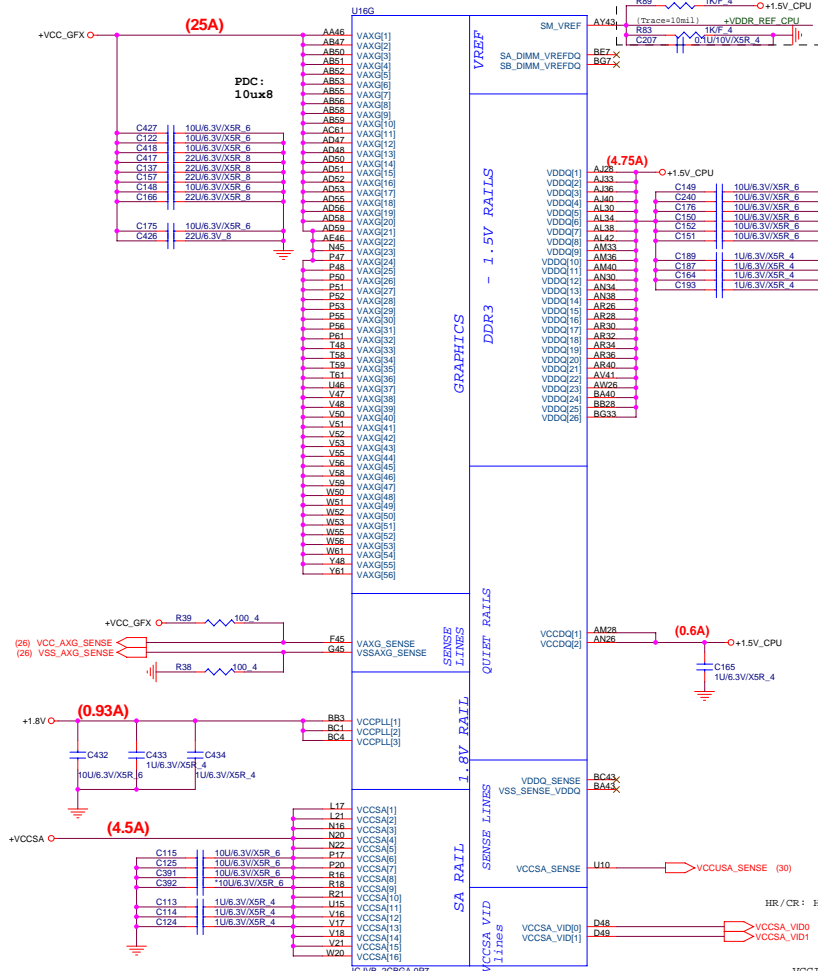
Date: Thursday, January 17, 2013 Sheet 5 of 41

## POWER

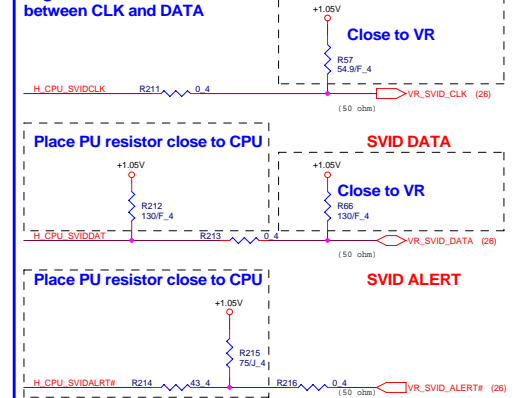
CPU Core Power



SNB:6A



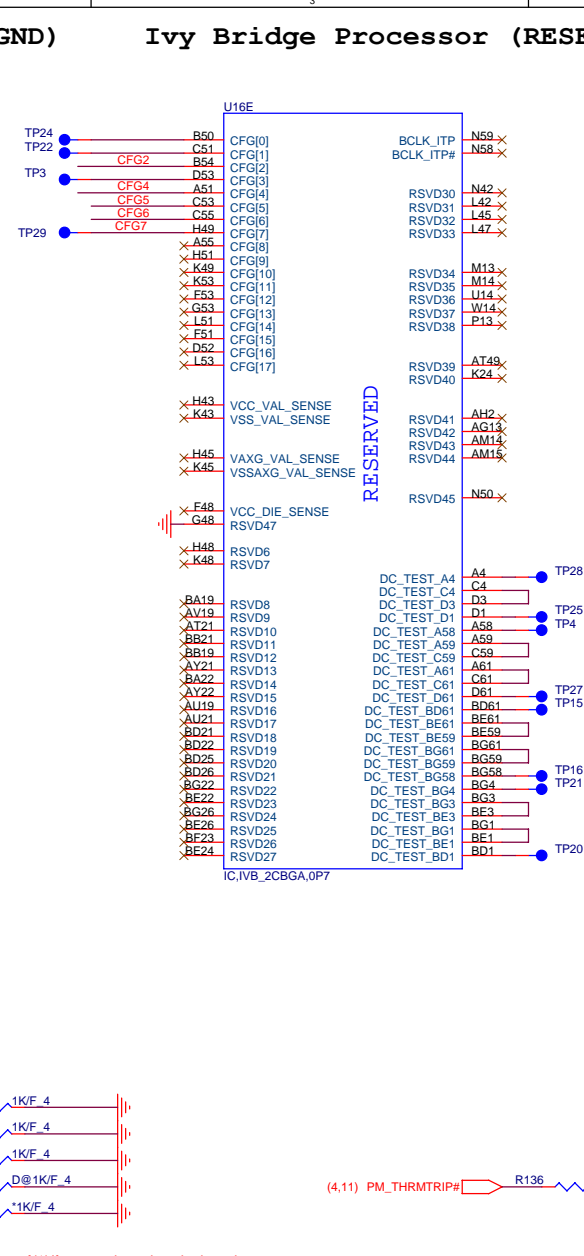
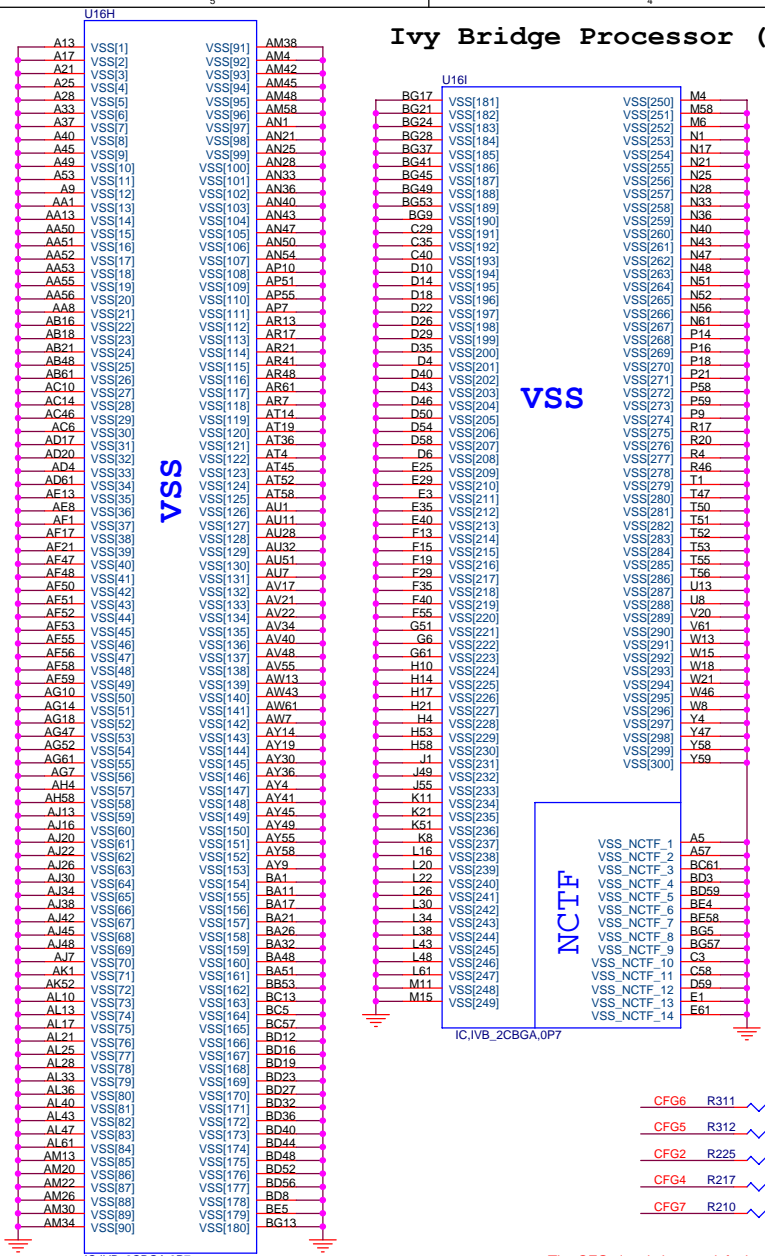
Layout note: need routing together and ALERT need between CLK and DATA



```
VCCIO_SEL:
Sandy is High = 1.05V
Ivy is Low = 1.0V
```

Ivy Bridge Processor (GND)

Ivy Bridge Processor (RESERVED, CFG)

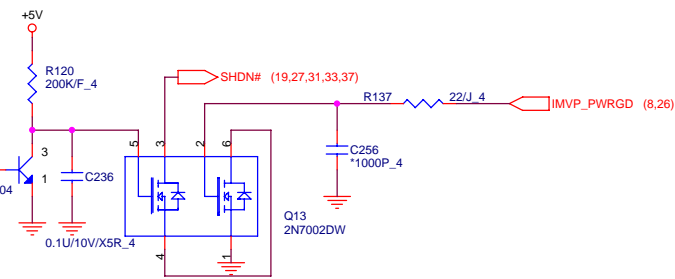



The CFG signals have a default value of '1' if not terminated on the board.

Processor Strapping

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

CFG[6:5] (PCIe Port Bifurcation Straps)  
11: (Default) x16 - X16 PEG interface  
10: PEG x8 x8 bifurcation enabledisabled  
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled  
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled





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CPT/PPT (LVDS, DDI)

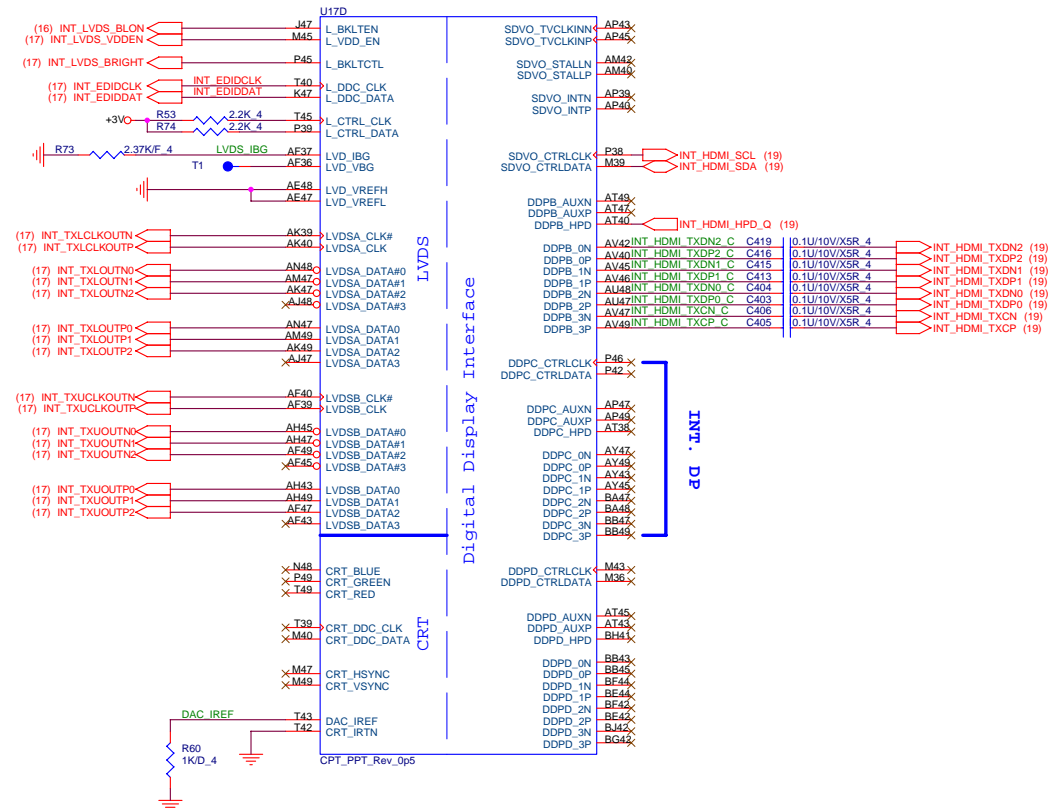


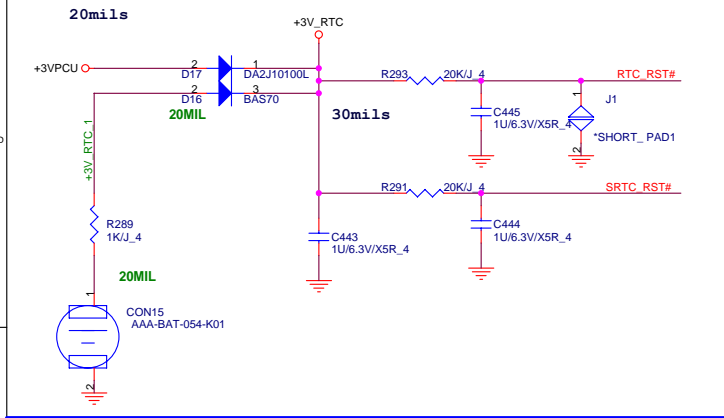
Figure 1: Schematic diagram of the PMIC configuration for the STM32MP157C-DK. The diagram shows the PMIC (PM8941) connected to the STM32MP157C-DK. The PMIC is configured with the following components:

- PM\_R1# (R267, 10K/J, 4)
- SUSWARN# (R108, 10K/J, 4)
- PM\_BATLOW# (R135, 8.2K/J, 4)
- AC\_PRESENT (R105, 10K/J, 4)
- PM\_DRAM\_PWRGD (R265, 200/F, 4)
- PCIE\_WAKE# (R269, 10K/J, 4)
- CLKRUN# (R148, 8.2K/J, 4)
- XDP\_DBRST# (R278, 1K/J, 4)
- PWROK\_R (R169, 47K, 4)
- 3V supply connection

On Die DSW VR Enable
High = Enable (Default)
Low = Disable

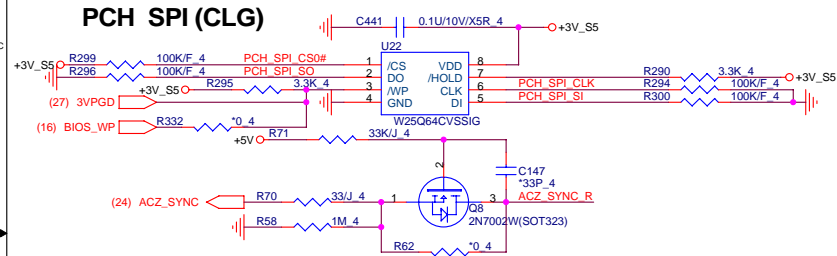


## RTC Circuitry(RTC)



MX25L3205DM2I-12G: AKE39FP0200  
W25X32VSSIG: AKE39ZP0N00

## PCH SPI (CLG)



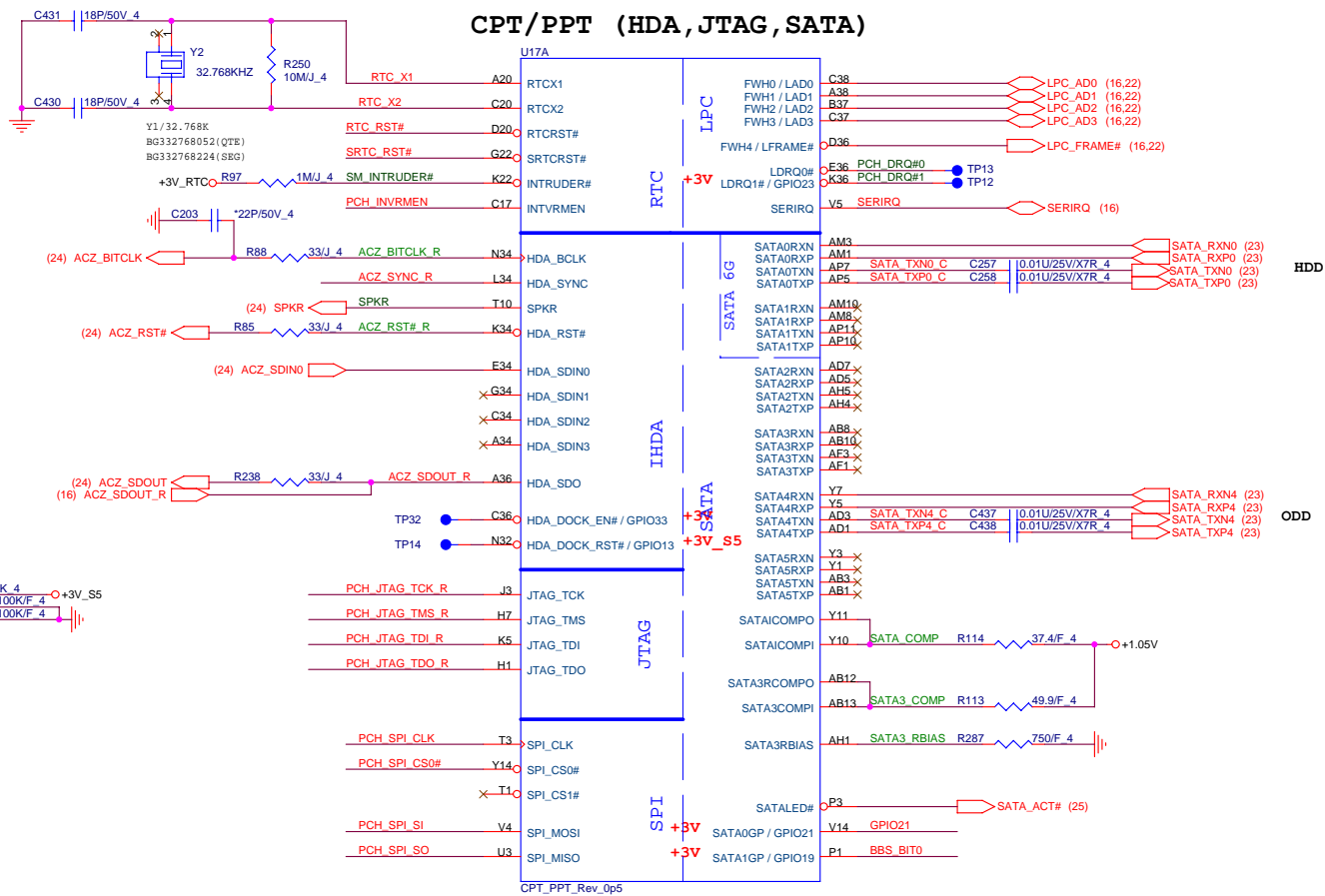
(16) F_CS0#_PCH	R298	0.4	PCH SPI CS0#
(16) F_SDI_PCH	R297	0.4	PCH SPI SO
(16) SCK_PCH	R292	0.4	PCH SPI CLK
(16) SD0_PCH	R301	0.4	PCH SPI SI

For NPCE885L Using

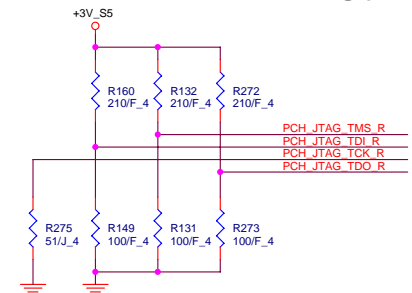
## PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Note									
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	SPKR									
PCI_GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	TP7  PCI_GNT3# (10)									
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC  R255  330K/J_4  PCH_INVRMEN									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table><tr><td>GNT1#</td><td>GNT0#</td><td>Boot Location</td></tr><tr><td>1</td><td>1</td><td>SPI *</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></table>	GNT1#	GNT0#	Boot Location	1	1	SPI *	0	0	LPC	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]
GNT1#	GNT0#	Boot Location											
1	1	SPI *											
0	0	LPC											
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	TP30  BBS_BIT1 (10) TP33  BBS_BIT0										
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Enabled	ACZ_SDOOUT_R									
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss for Ivy Bridge 1 = Set to Vcc for Sandy Bridge (weak pull-down 20K)	R282  2.2K_4  +1.8V R276  1K/J_4  NV_CLE (11) H_SNB_IVB# (4)									
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	TP19  PLL_ODVR_EN (11)									
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5  R65  1K/J_4  ACZ_SYNC_R									

## CPT/PPT (HDA, JTAG, SATA)



## PCH JTAG Debug (CLG)



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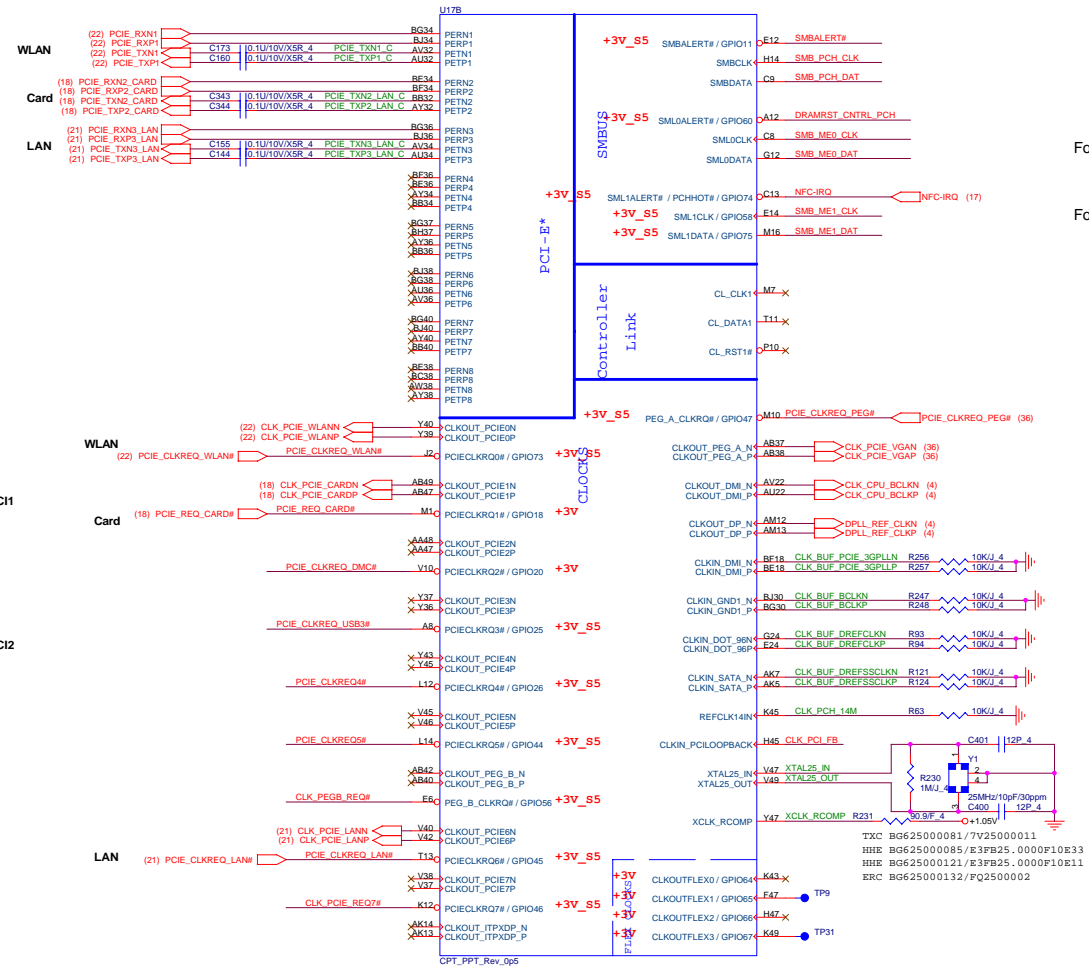
Size: Document Number: CPT/PPT 2/6 Rev 1A

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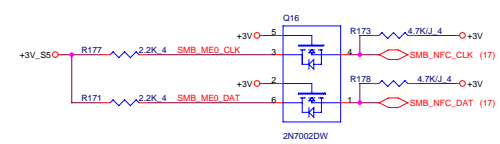
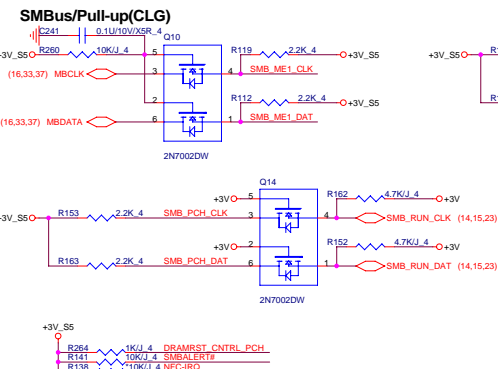
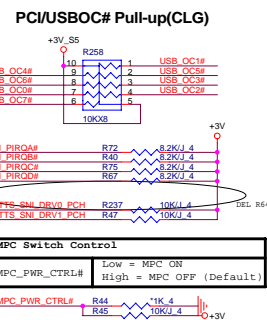
1. Level 1 Environment-related Substances Should Never be Used.

2. Recycled Resin and Coated Wire should be procured from Green Partners.

CPT/PPT (PCI-E, SMBUS, CLK)



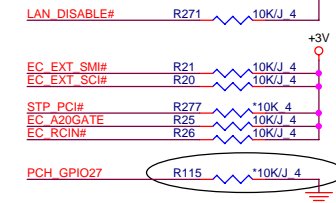
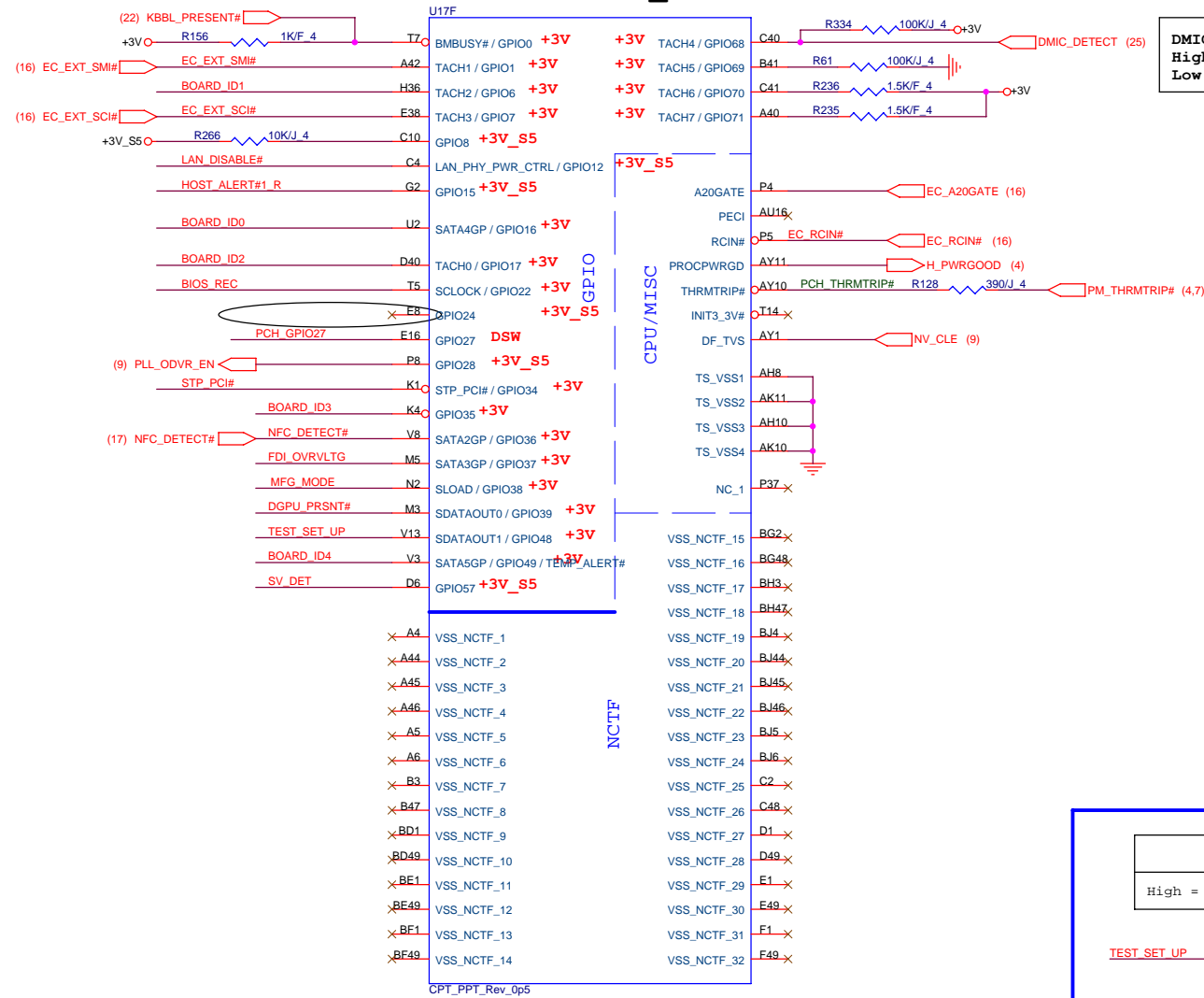
For EC



## CPT/PPT (GPIO,VSS\_NCTF,RSVD)

## GPIO Pull-up/Pull-down(CLG)

11



	0	1
Board ID0	CaspiCRA1-CaspiCRB1 HK8-HK9	SuperiorCRA1-SuperiorCRB1 GD5-GD6
Board ID1	HK8/GD5 14"	HK9/GD6 15"

SV\_SET\_UP

High = Strong (Default)

TEST\_SET\_UP → R143 → 10K/J 4 → +3V

HOST\_ALERT#1\_R → R270 → 1K/J 4 → +3V\_S5

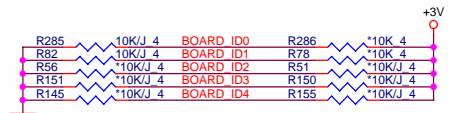
Intel ME Crypto Transport Layer Security (TLS) cipher suite

Low = Disable (Default)

High = Enable

## MFG-TEST

MFG\_MODE → R281 → 10K/J 4 → +3V



PCBA SKU	Discrete	UMA
R280(Pull High)	Stuff	No Stuff
R279(Pull Low)	No Stuff	Stuff

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CPT/PPT 4/6

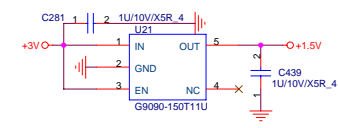
Size: Document Number

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## U17J POWER

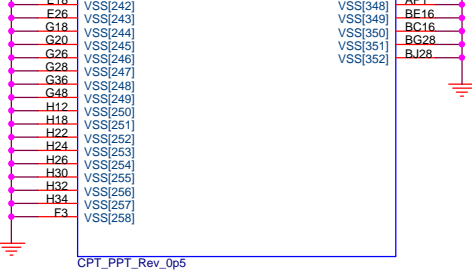


CPT/PPT (GND)


U17H		
H5	VSS[0]	
AA17	VSS[1]	VSS[80]
AA2	VSS[2]	
AA3	VSS[3]	
AA33	VSS[4]	
AA34	VSS[5]	
AB11	VSS[6]	
AB14	VSS[7]	
AB38	VSS[8]	
AB4	VSS[9]	
AB43	VSS[10]	
AB5	VSS[11]	
AB7	VSS[12]	
AC19	VSS[13]	
AC2	VSS[14]	
AC21	VSS[15]	
AC24	VSS[16]	
AC33	VSS[17]	
AC34	VSS[18]	
AC48	VSS[19]	
AD10	VSS[20]	
AD11	VSS[21]	
AD12	VSS[22]	
AD13	VSS[23]	
AD19	VSS[24]	
AD24	VSS[25]	
AD26	VSS[26]	
AD27	VSS[27]	
AD33	VSS[28]	
AD34	VSS[29]	
AD36	VSS[30]	
AD37	VSS[31]	
AD38	VSS[32]	
AD39	VSS[33]	
AD4	VSS[34]	
AD40	VSS[35]	
AD42	VSS[36]	
AD43	VSS[37]	
AD45	VSS[38]	
AD46	VSS[39]	
AD8	VSS[40]	
AE2	VSS[41]	
AE3	VSS[42]	
AF10	VSS[43]	
AF12	VSS[44]	
AD14	VSS[45]	
AD16	VSS[46]	
AF16	VSS[47]	
AF19	VSS[48]	
AF24	VSS[49]	
AF26	VSS[50]	
AF27	VSS[51]	
AF29	VSS[52]	
AF31	VSS[53]	
AF38	VSS[54]	
AF4	VSS[55]	
AF42	VSS[56]	
AF46	VSS[57]	
AF5	VSS[58]	
AF7	VSS[59]	
AF8	VSS[60]	
AG19	VSS[61]	
AG2	VSS[62]	
AG31	VSS[63]	
AG48	VSS[64]	
AH11	VSS[65]	
AH3	VSS[66]	
AH36	VSS[67]	
AH39	VSS[68]	
AH40	VSS[69]	
AH42	VSS[70]	
AH46	VSS[71]	
AH7	VSS[72]	
AJ19	VSS[73]	
AJ21	VSS[74]	
AJ24	VSS[75]	
AJ33	VSS[76]	
AJ34	VSS[77]	
AK12	VSS[78]	
AK3	VSS[79]	



U17I		
AY4	VSS[159]	
AY42	VSS[160]	
AY46	VSS[161]	
AY8	VSS[162]	
B11	VSS[163]	
B15	VSS[164]	
B19	VSS[165]	
B23	VSS[166]	
B27	VSS[167]	
B31	VSS[168]	
AL17	VSS[169]	
AL19	VSS[170]	
B7	VSS[171]	
F45	VSS[172]	
BB12	VSS[173]	
BB16	VSS[174]	
BB20	VSS[175]	
BB22	VSS[176]	
BB24	VSS[177]	
BB28	VSS[178]	
BB30	VSS[179]	
BB38	VSS[180]	
BB4	VSS[181]	
BB46	VSS[182]	
BC14	VSS[183]	
BC18	VSS[184]	
BC2	VSS[185]	
BC22	VSS[186]	
BC26	VSS[187]	
AN2	VSS[188]	
BC32	VSS[189]	
BC34	VSS[190]	
BC36	VSS[191]	
BC40	VSS[192]	
BC42	VSS[193]	
AP19	VSS[194]	
AP28	VSS[195]	
BD5	VSS[196]	
BE22	VSS[197]	
BE26	VSS[198]	
AP4	VSS[199]	
AP42	VSS[200]	
BF12	VSS[201]	
BF16	VSS[202]	
BF20	VSS[203]	
BF22	VSS[204]	
BF24	VSS[205]	
BF28	VSS[206]	
BD3	VSS[207]	
BF30	VSS[208]	
BF38	VSS[209]	
BF40	VSS[210]	
BF8	VSS[211]	
AT34	VSS[212]	
BG17	VSS[213]	
BG21	VSS[214]	
BG33	VSS[215]	
BG44	VSS[216]	
BG8	VSS[217]	
BH11	VSS[218]	
AU24	VSS[219]	
AU30	VSS[220]	
BH17	VSS[221]	
BH19	VSS[222]	
H10	VSS[223]	
BH27	VSS[224]	
BH31	VSS[225]	
AV4	VSS[226]	
BH33	VSS[227]	
BH35	VSS[228]	
BH39	VSS[229]	
BH43	VSS[230]	
BH7	VSS[231]	
AW2	VSS[232]	
D12	VSS[233]	
D16	VSS[234]	
D18	VSS[235]	
D22	VSS[236]	
D24	VSS[237]	
D26	VSS[238]	
AW40	VSS[239]	
D32	VSS[240]	
D34	VSS[241]	
D38	VSS[242]	
D42	VSS[243]	
D8	VSS[244]	
E18	VSS[245]	
E26	VSS[246]	
G18	VSS[247]	
G20	VSS[248]	
G26	VSS[249]	
G28	VSS[250]	
G36	VSS[251]	
G48	VSS[252]	
H12	VSS[253]	
H18	VSS[254]	
H22	VSS[255]	
H24	VSS[256]	
H26	VSS[257]	
H30	VSS[258]	
H32		
H34		
F3		



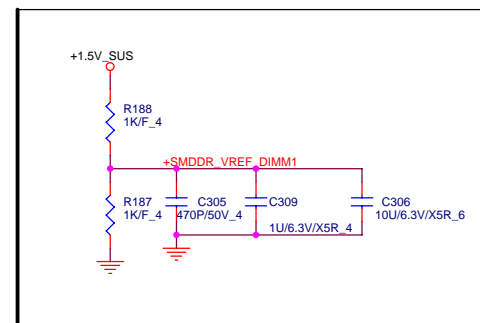
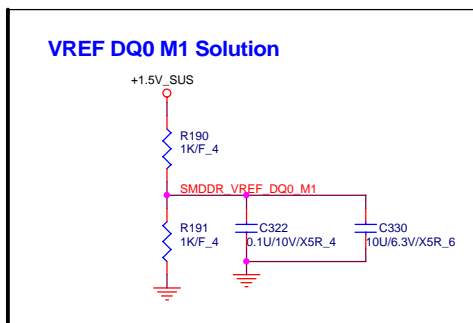
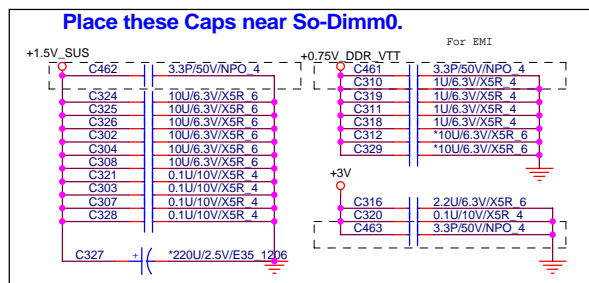
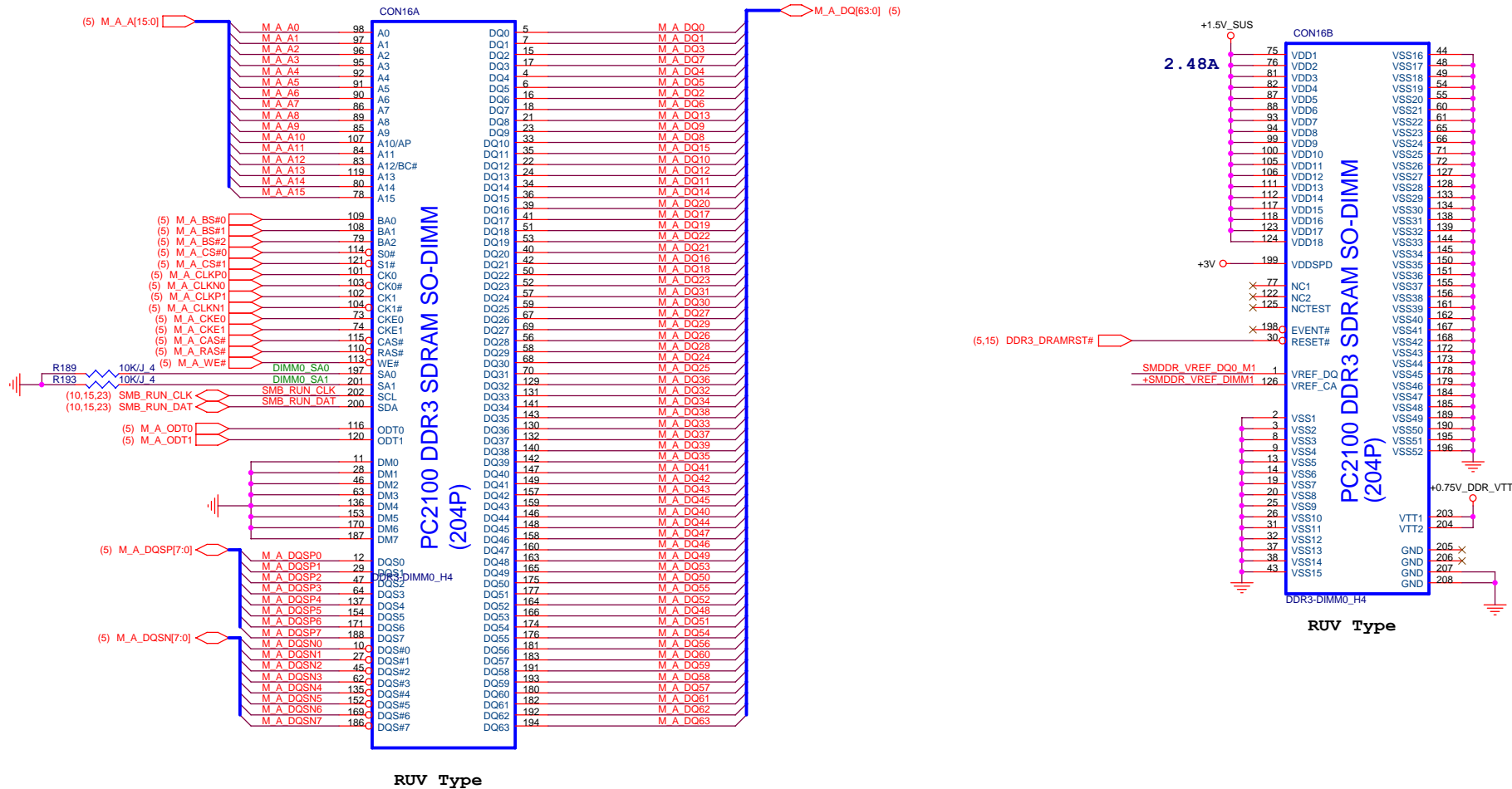
VSS[259]	H46
VSS[260]	K18
VSS[261]	K26
VSS[262]	K39
VSS[263]	K46
VSS[264]	K7
VSS[265]	L18
VSS[266]	L2
VSS[267]	L20
VSS[268]	L26
VSS[269]	L28
VSS[270]	L36
VSS[271]	L48
VSS[272]	M12
VSS[273]	P16
VSS[274]	M18
VSS[275]	M22
VSS[276]	M24
VSS[277]	M30
VSS[278]	M32
VSS[279]	M34
VSS[280]	M38
VSS[281]	M4
VSS[282]	M42
VSS[283]	M46
VSS[284]	M8
VSS[285]	N18
VSS[286]	P30
VSS[287]	N47
VSS[288]	P41
VSS[289]	P18
VSS[290]	T33
VSS[291]	P40
VSS[292]	P43
VSS[293]	P47
VSS[294]	P7
VSS[295]	R2
VSS[296]	R48
VSS[297]	T12
VSS[298]	T31
VSS[299]	T37
VSS[300]	T4
VSS[301]	V34
VSS[302]	T46
VSS[303]	T47
VSS[304]	T8
VSS[305]	V11
VSS[306]	V17
VSS[307]	V26
VSS[308]	V27
VSS[309]	V29
VSS[310]	V31
VSS[311]	V36
VSS[312]	V39
VSS[313]	V43
VSS[314]	V7
VSS[315]	W17
VSS[316]	W19
VSS[317]	W2
VSS[318]	W27
VSS[319]	W48
VSS[320]	Y12
VSS[321]	Y38
VSS[322]	Y4
VSS[323]	Y42
VSS[324]	Y46
VSS[325]	Y8
VSS[326]	BG29
VSS[327]	N24
VSS[328]	AJ3
VSS[329]	AD47
VSS[330]	B43
VSS[331]	BE10
VSS[332]	BG41
VSS[333]	G14
VSS[334]	H16
VSS[335]	T36
VSS[336]	BG22
VSS[337]	BG24
VSS[338]	C22
VSS[339]	AP13
VSS[340]	M14
VSS[341]	AP3
VSS[342]	AP1
VSS[343]	BE16
VSS[344]	BC16
VSS[345]	BG28
VSS[346]	BJ28
VSS[347]	
VSS[348]	
VSS[349]	
VSS[350]	
VSS[351]	
VSS[352]	



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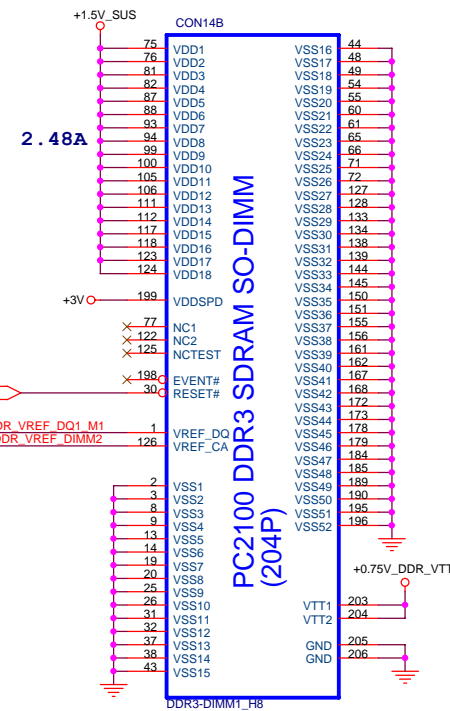
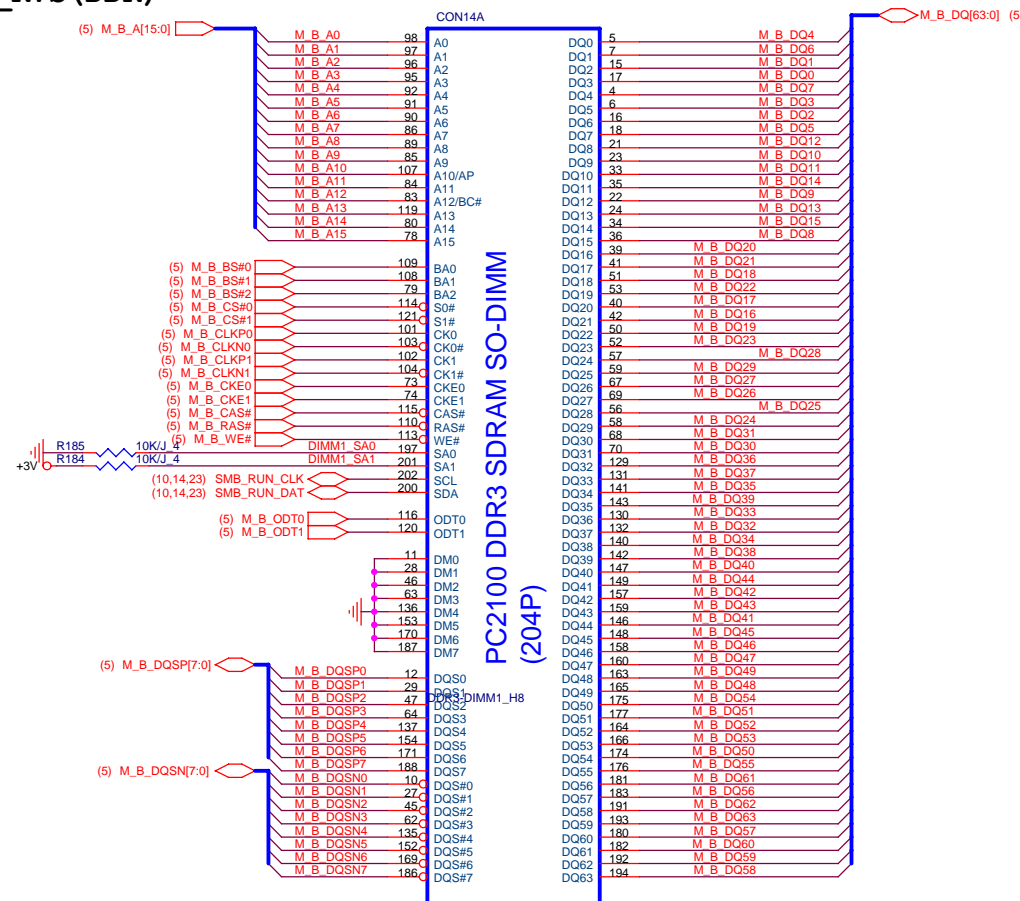
PROJECT :Chief River

Size	Document Number	CPT/PPT 6/6	Rev 1A
1.Level 1 Environment-related Substances Should Never be Used.		Date: Thursday, January 17, 2013	Sheet 13 of 41
2.Recycled Resin and Coated Wire should be procured from Green Partners.			



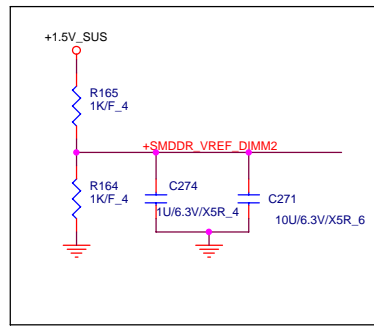
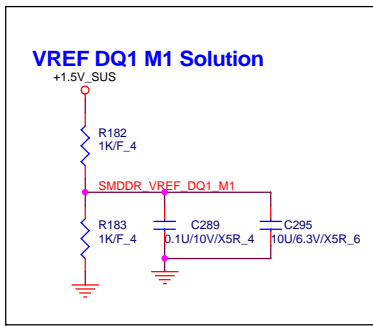
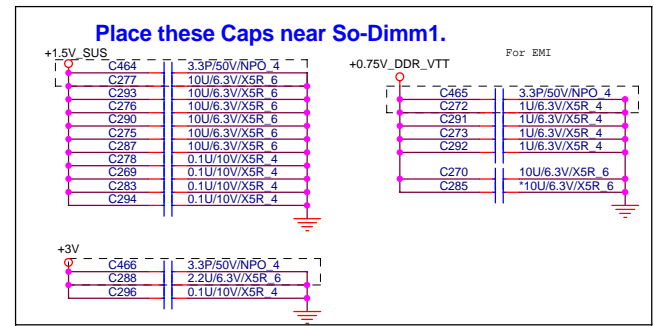


# DDR\_RVS (DDR)



15

RUV Type



Quanta Computer Inc.

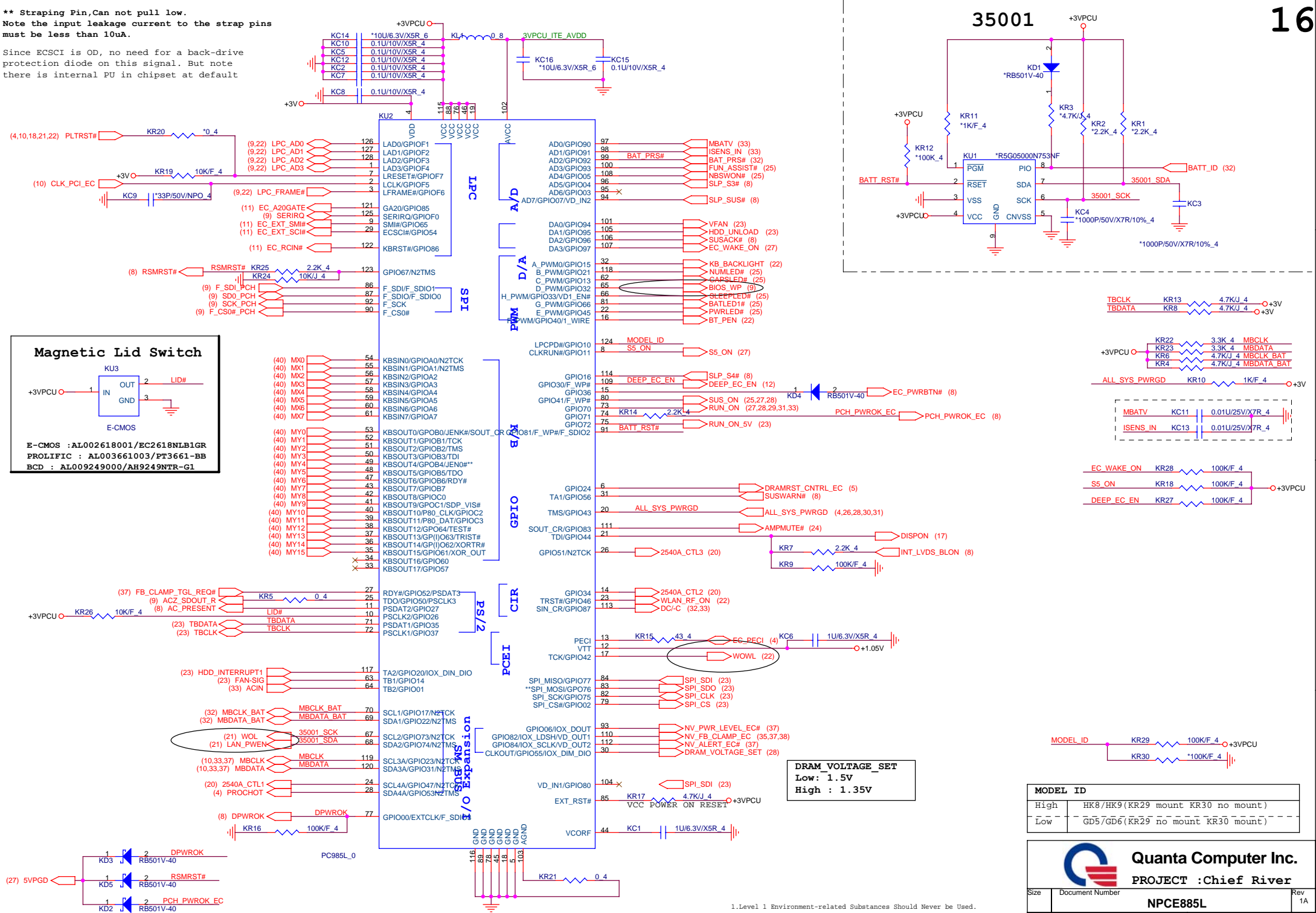
PROJECT :Chief River

DDRIII SO-DIMM-1

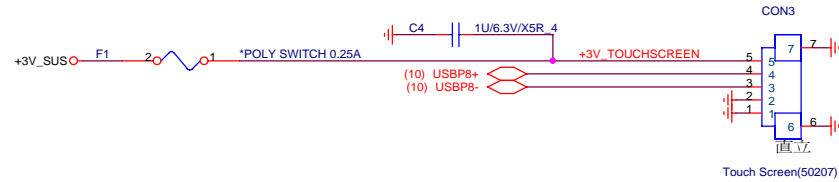
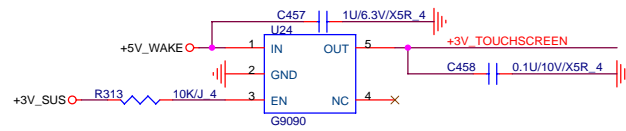
Size	Document Number	Date	Thursday, January 17, 2013	Sheet	15	of	41	Rev	1A
<p>1.Level 1 Environment-related Substances Should Never be Used.</p> <p>2.Recycled Resin and Coated Wire should be procured from Green Partners.</p>									



Since ECSCI is OD, no need for a back-drive protection diode on this signal. But note there is internal PU in chipset at default



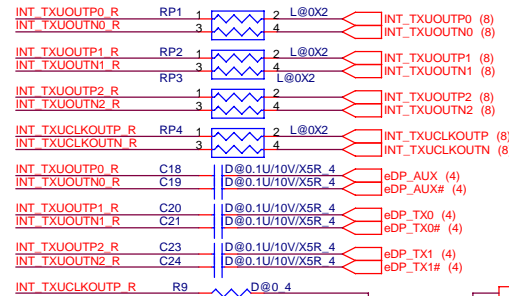
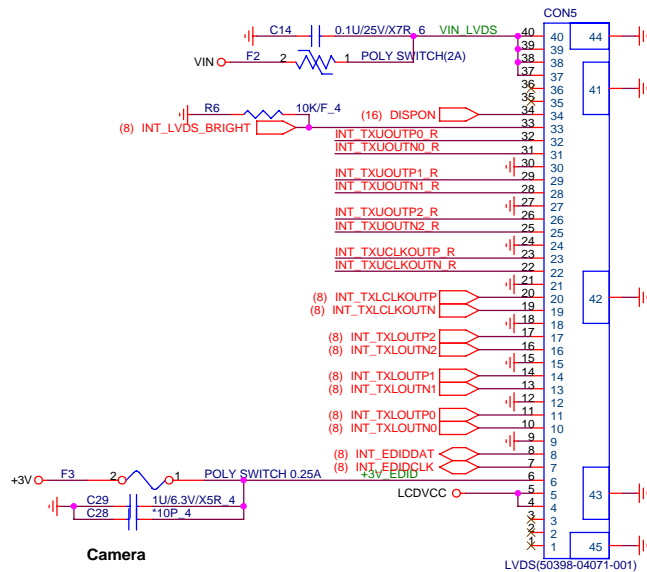
## Touch Screen



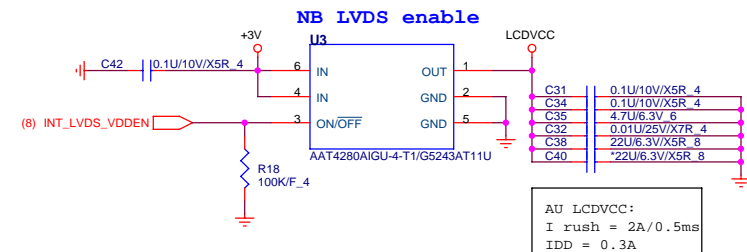
NFC module :  
Vender : Samsung SNC-i20  
Power consumption : Max. 160mW/48mA  
Power Ripple +/- 50mV

FAST, UL/CSA

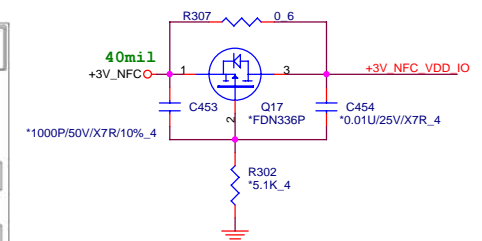
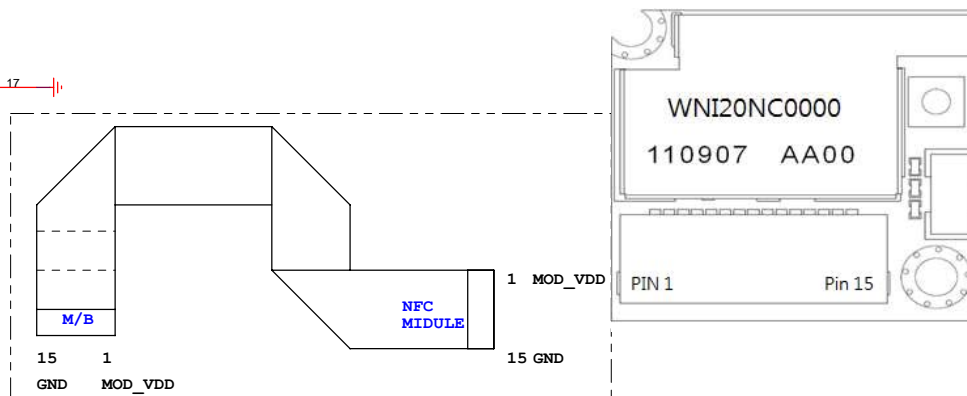
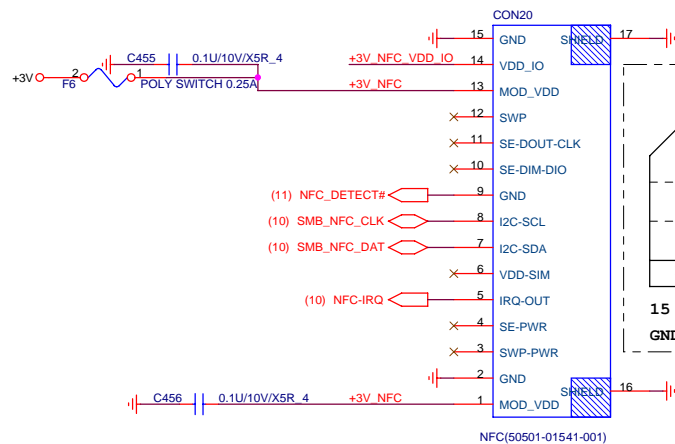
## LVDS



Camera HD specification  
Voltage: Max. 3.6V  
Current : Max. 200mA  
OCP: 200mA ~ 300mA



## NFC



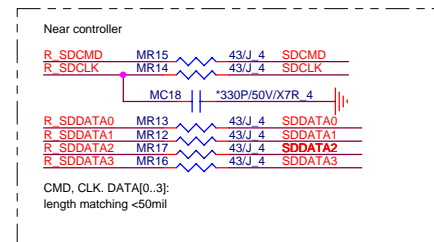
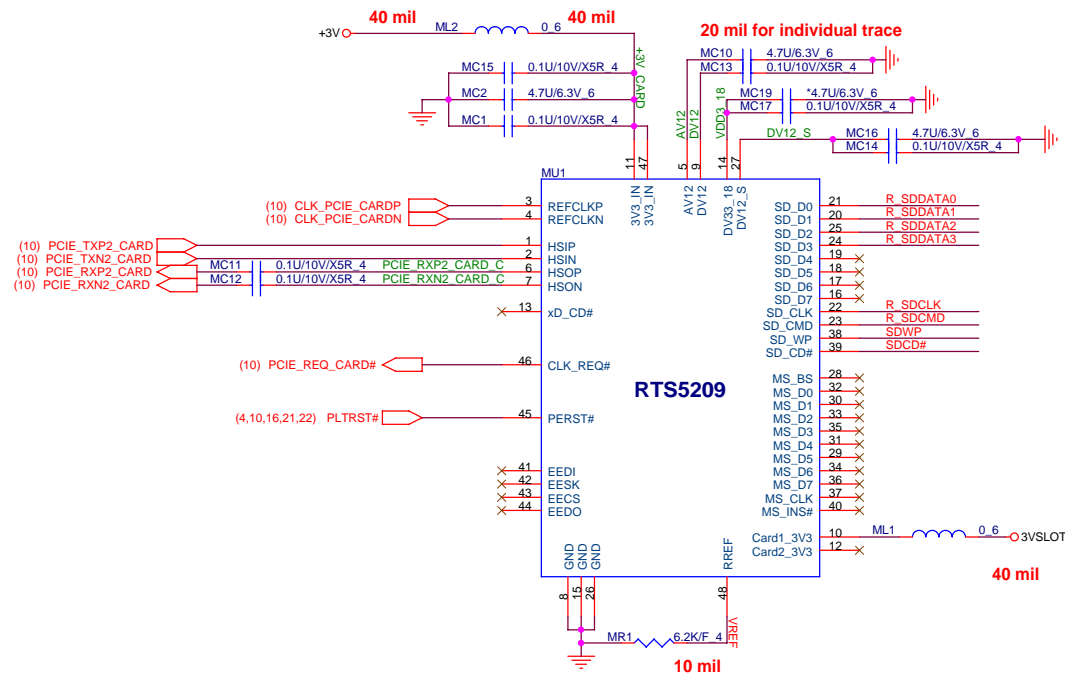
Quanta Computer Inc.

PROJECT :Chief River

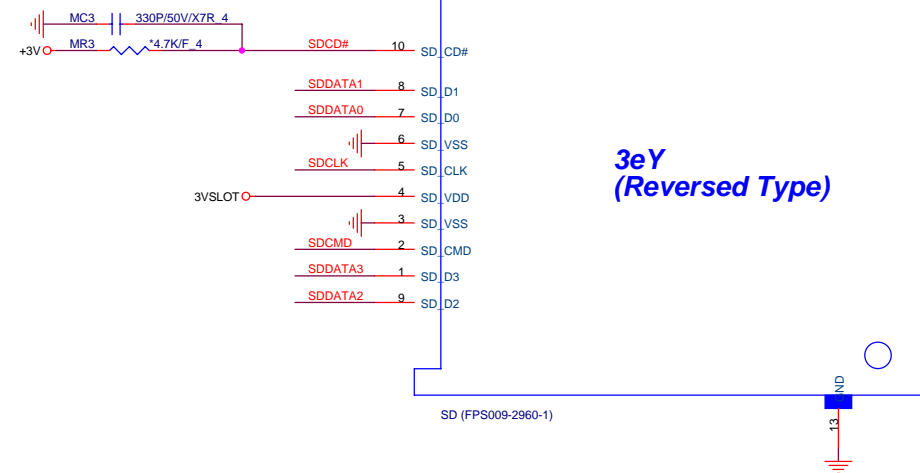
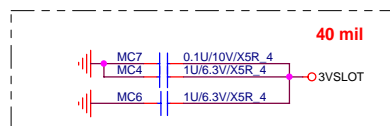
Size	Document Number	Rev
	CRT/LVDS	1A

1.Level 1 Environment-related Substances Should Never be Used.  
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Date: Thursday, January 17, 2013 Sheet 17 of 41

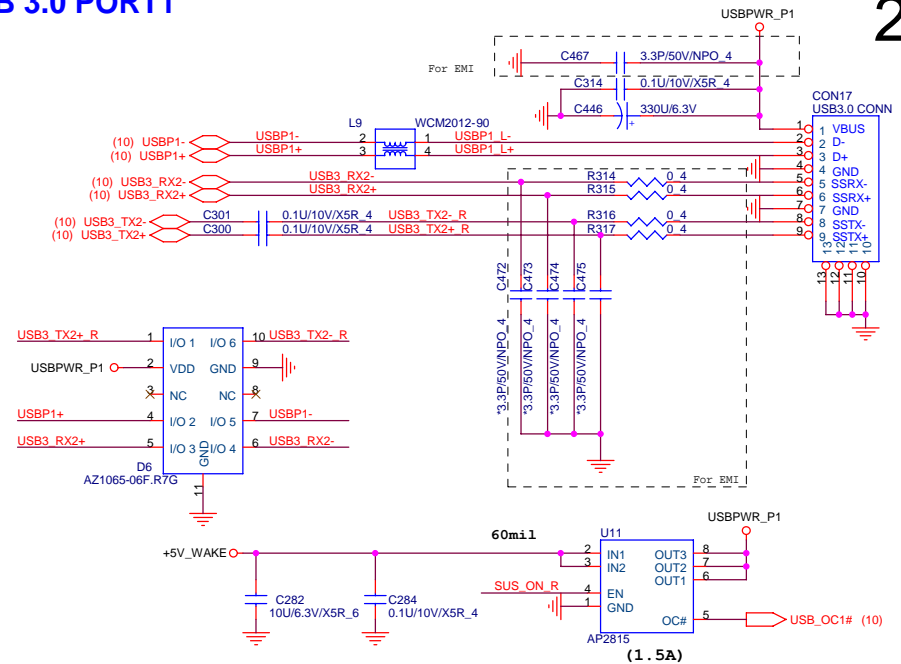


These component need  
to close to Slot

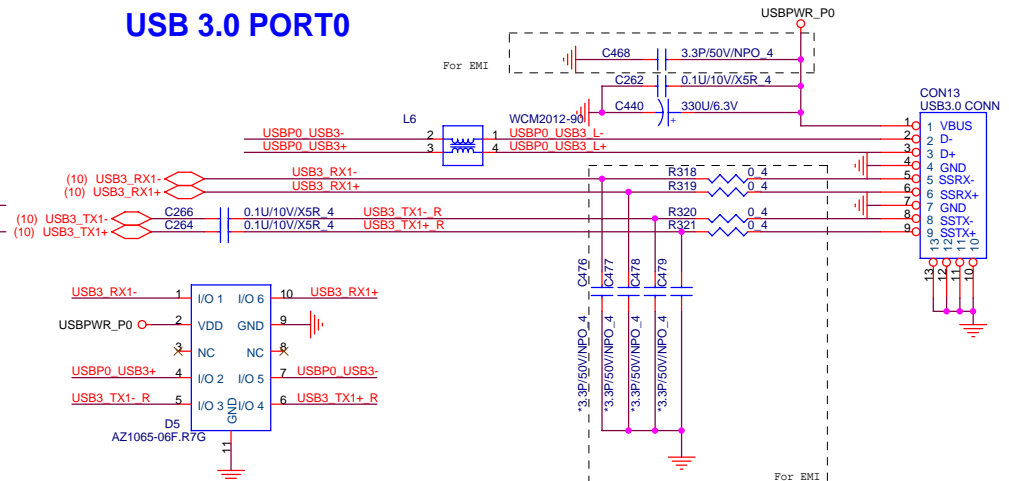


3eY  
(Reversed Type)






## USB 3.0 PORT0

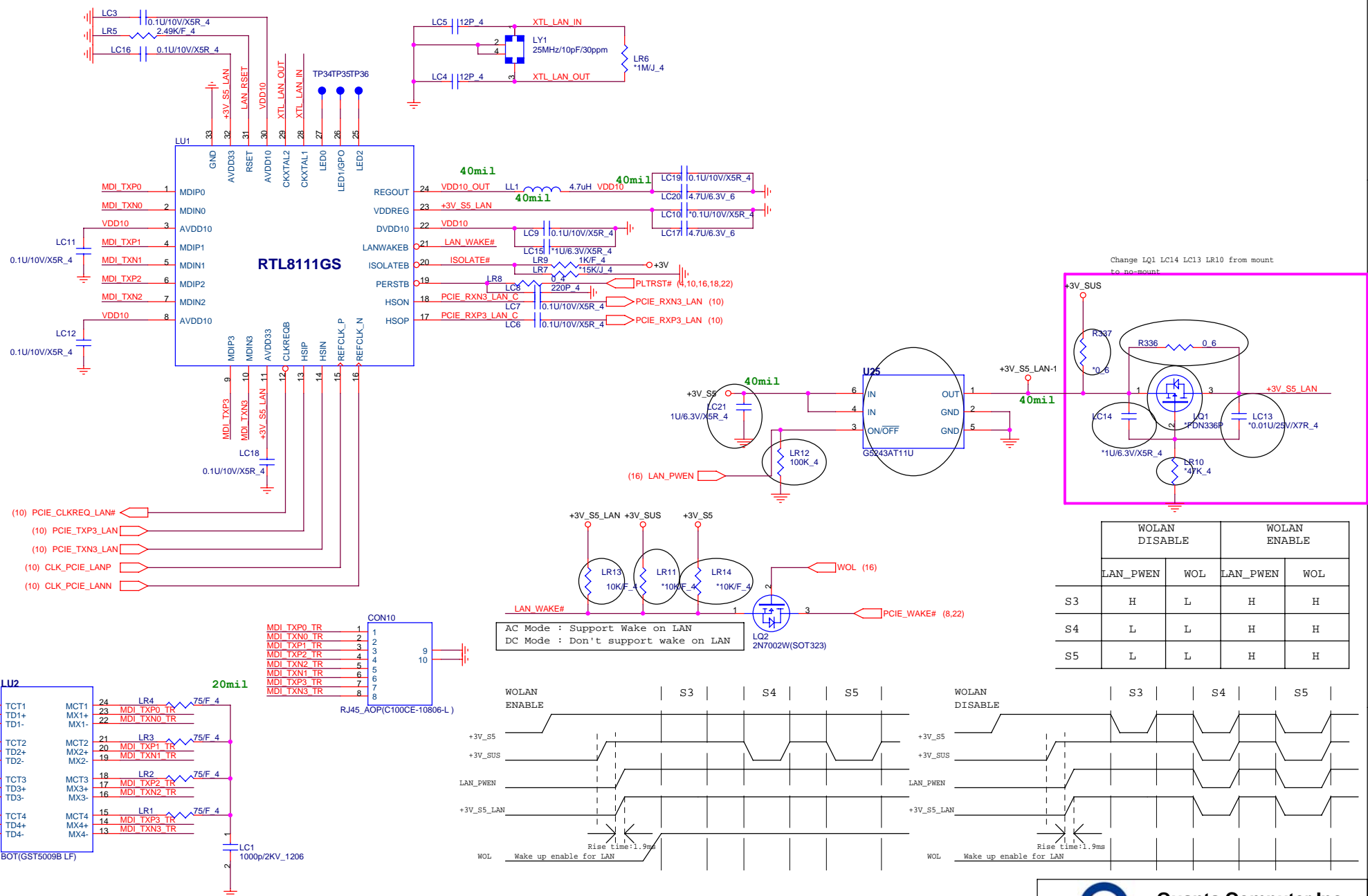


The diagram shows the relationship between the Mode signal and the VBUS signal. The Mode signal transitions from CDP to OFF and then to DCP. The VBUS signal transitions from high to low at the start of the OFF mode and returns to high at the end of the DCP mode. A double-headed arrow indicates the duration of the VBUS stop time, which is 1 second, occurring while the Mode signal is in the OFF state.

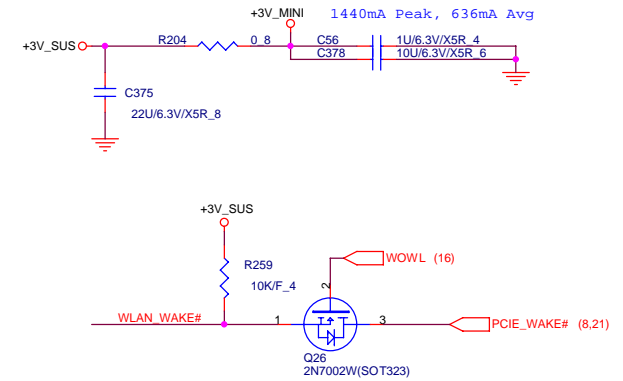
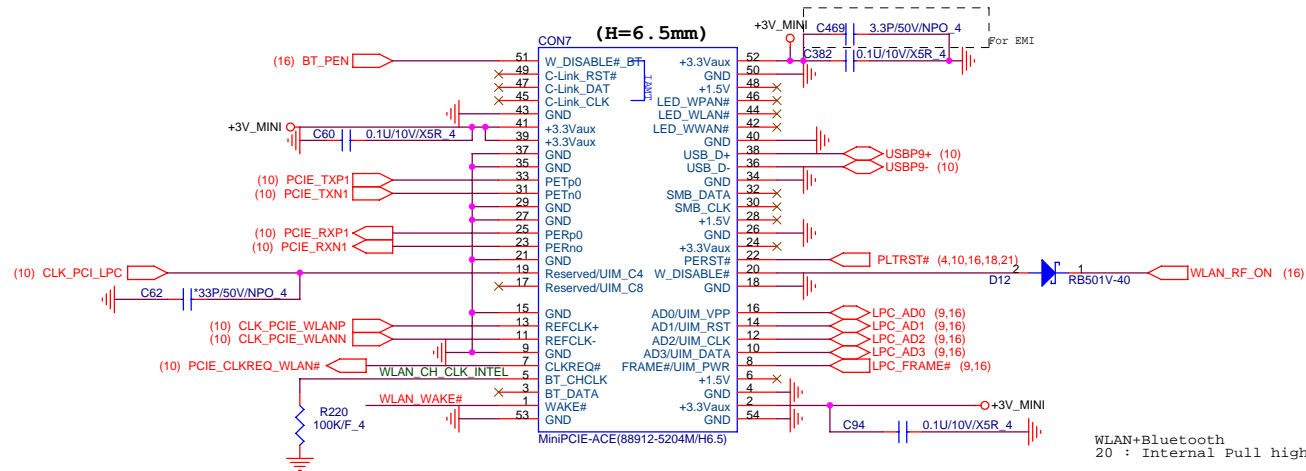
System State	USB Battery Charging Setting			
	Disable	C(1 2 3)	Enable	C(1 2 3)
S0	SDP	(X 1 0)	CDP	(1 1 1)
S3	SDP	(X 1 0)	DCP BC	(1 0 0)
DS3	Charger OFF	(0 0 0)	DCP BC	(1 0 0)
S4	Charger OFF	(0 0 0)	DCP BC	(1 0 0)
S5	Charger OFF	(0 0 0)	DCP BC	(1 0 0)

ILIM_SEL (I LIMIT(A)= 48000/R)		
HI	I_LIM_1	
LO	I_LIM_0	48000/22.6K=2.123A

 <b>Quanta Computer Inc.</b> <b>PROJECT :Chief River</b>		
<b>USB/USB Charger</b>		Rev 1A
Size	Document Number	
Date:	Thursday, January 17, 2013	Sheet 20 of 41

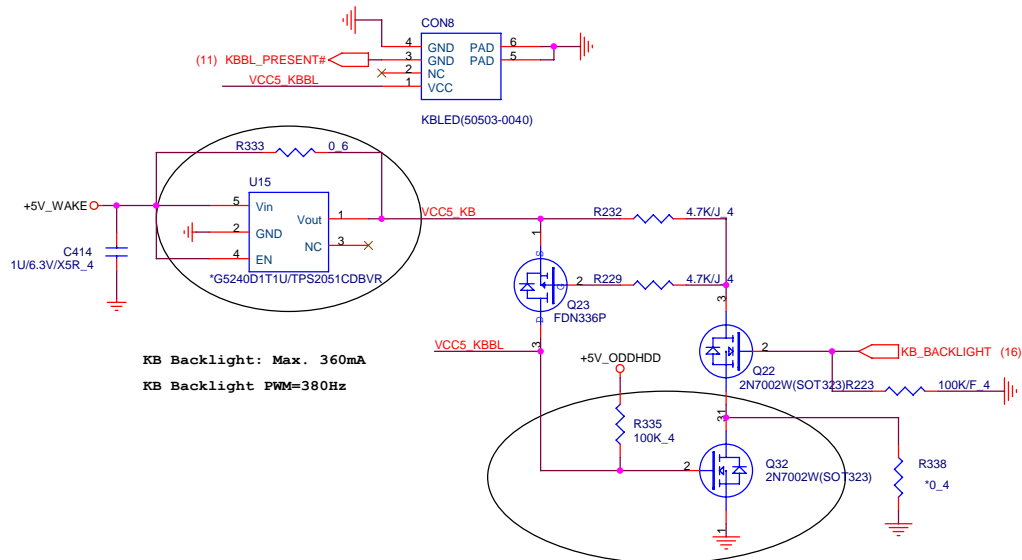


## WLAN/WIMAX/WIDI



AC Mode : Support Wake on WLAN  
DC Mode : Don't support wake on WLAN

## KB BACKLIGHT



Quanta Computer Inc.

PROJECT :Chief River

Size	Document Number	Rev
	WLAN/KB BL	1A

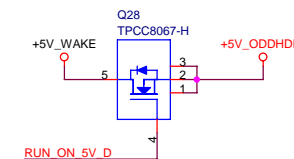
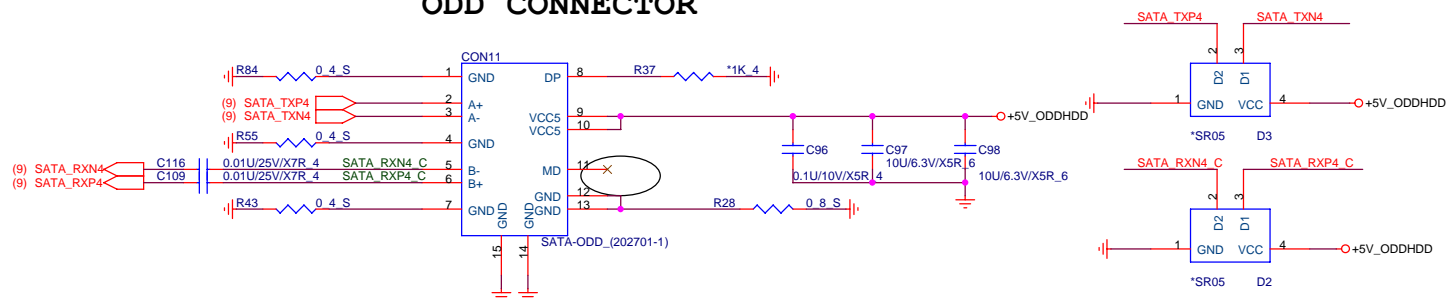
1.Level 1 Environment-related Substances Should Never be Used.

2.Recycled Resin and Coated Wire should be procured from Green Partners.

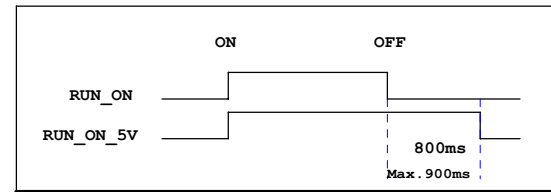
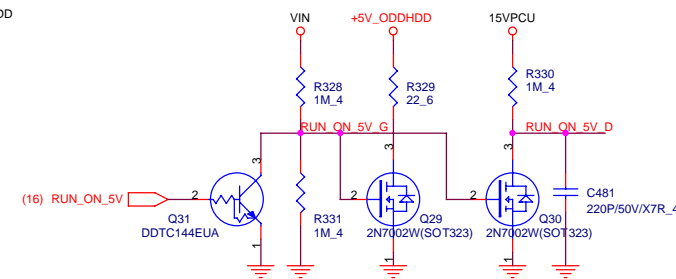
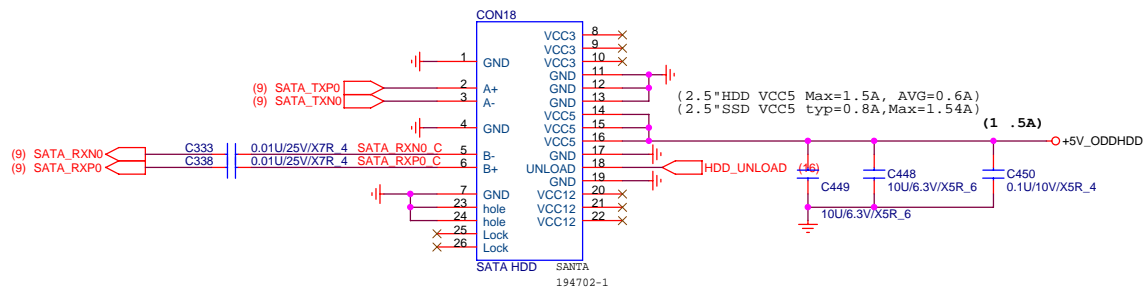
Date: Thursday, January 17, 2013 Sheet 22 of 41



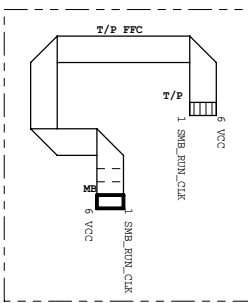
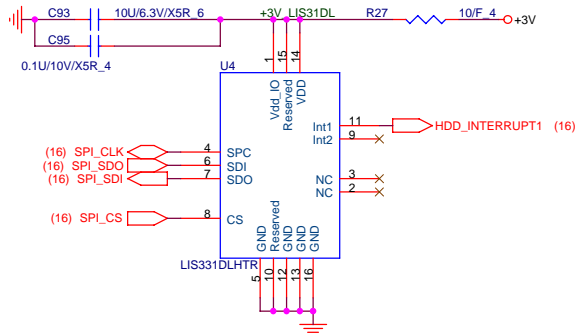
## ODD CONNECTOR



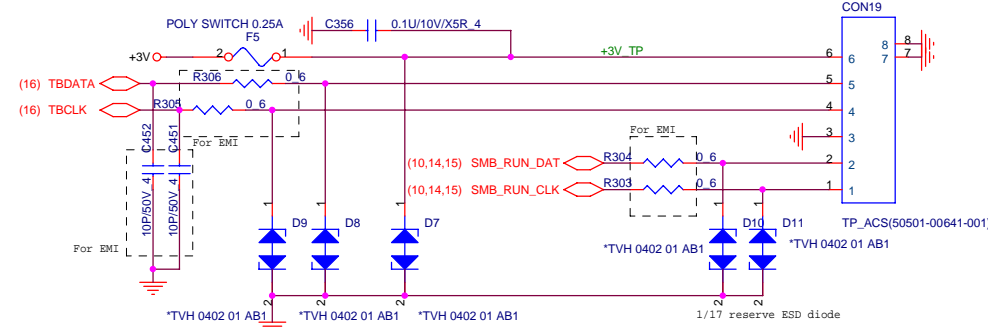
## HDD CONNECTOR



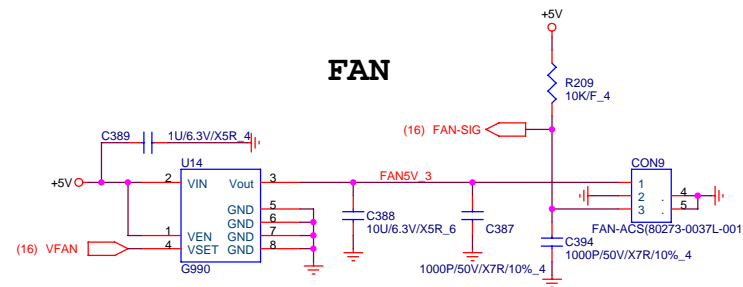
## HDD PROTECT SPI INTERFACE



## T/P Board to T/P



## FAN

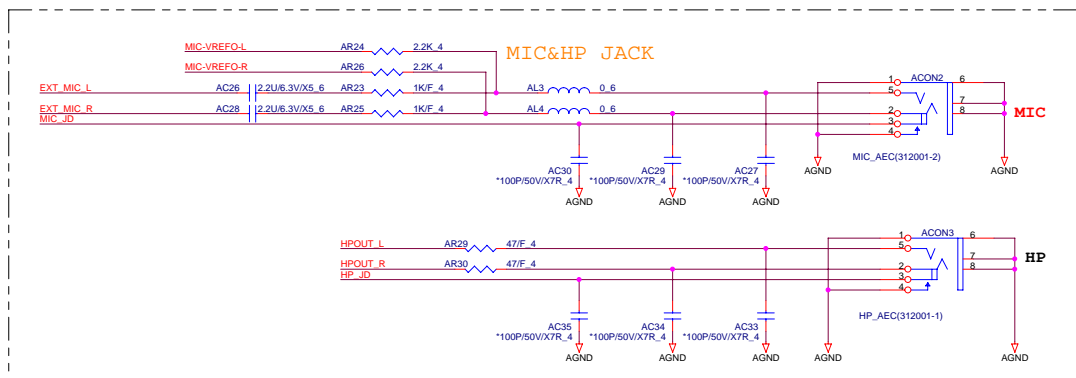
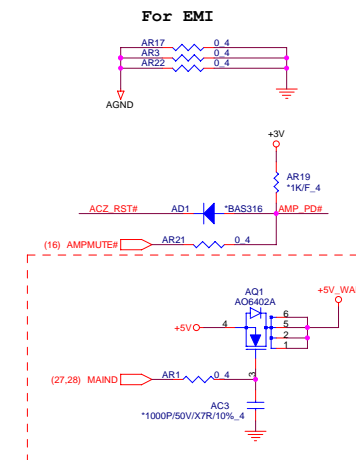
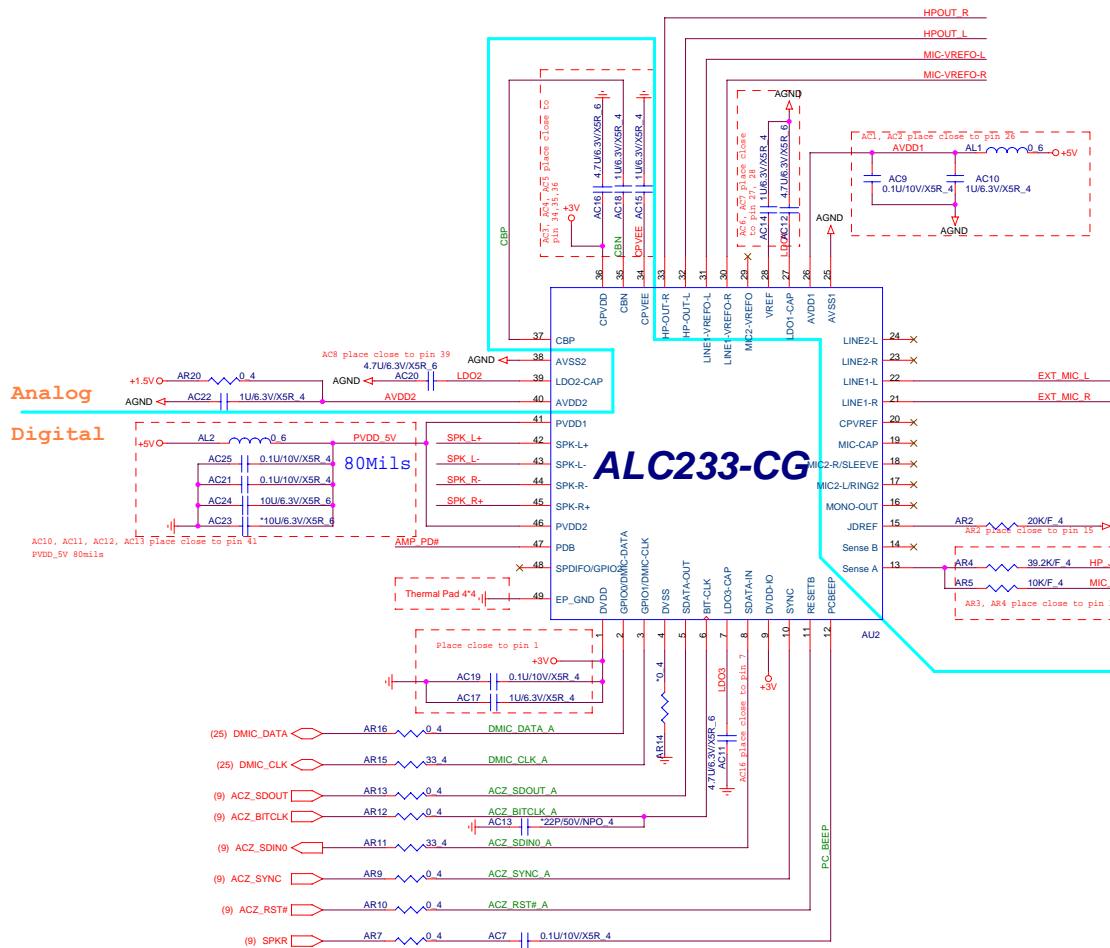


Quanta Computer Inc.  
PROJECT :Chief River

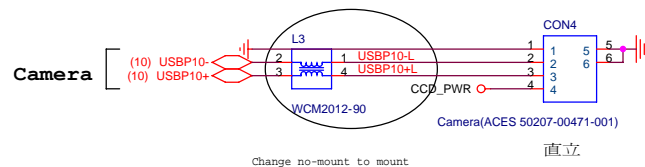
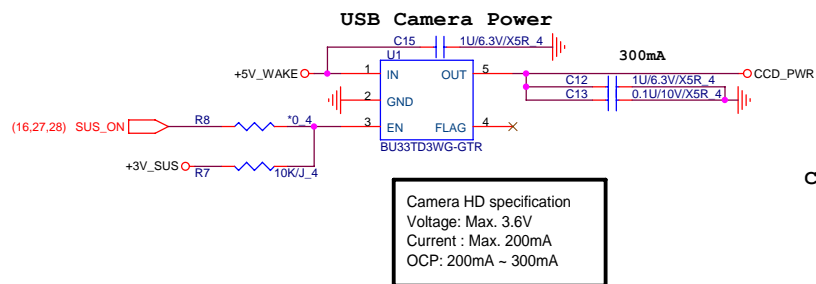
Size	Document Number	Rev
	HDD/ODD/TP/FAN	1A

1.Level 1 Environment-related Substances Should Never be Used.  
2.Recycled Resin and Coated Wire should be procured from Green Partners.

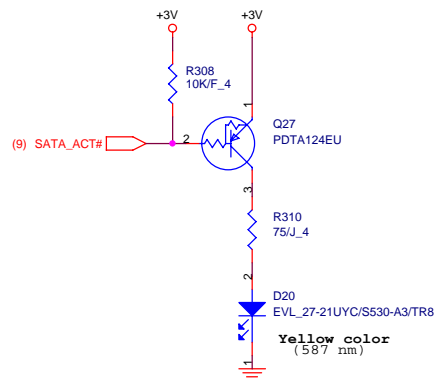
Date: Thursday, January 17, 2013 Sheet 23 of 41



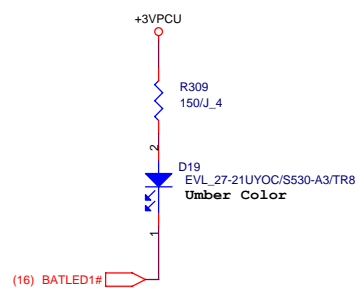
## Camera



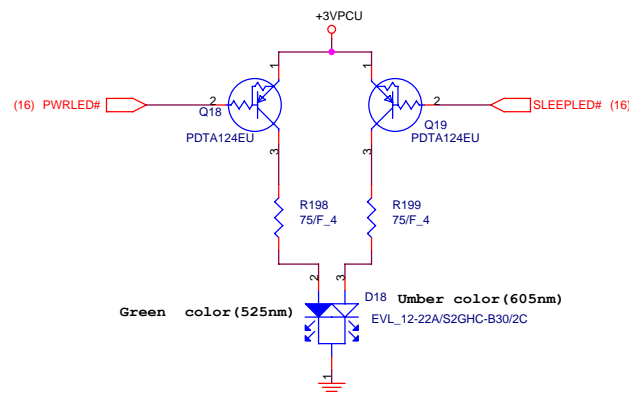
**SATA LED**



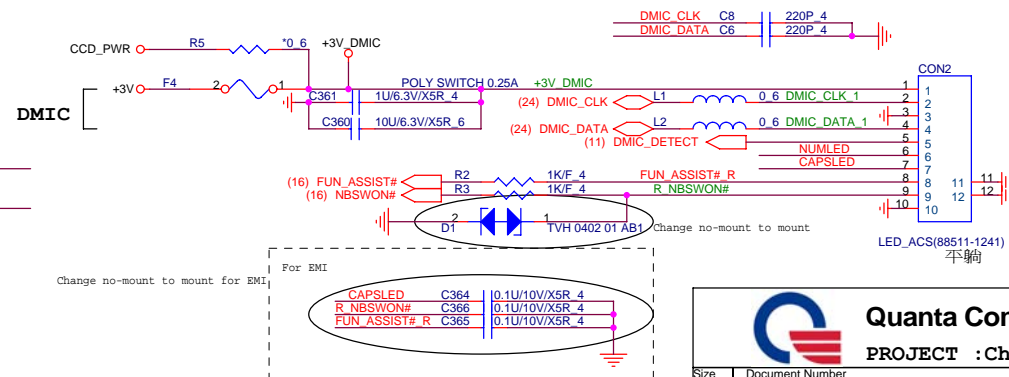
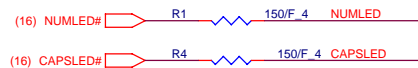
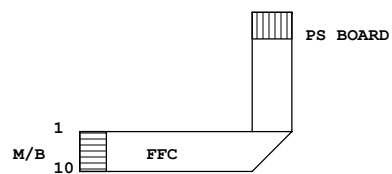
BATTERY LED



## Power/Sleep LED

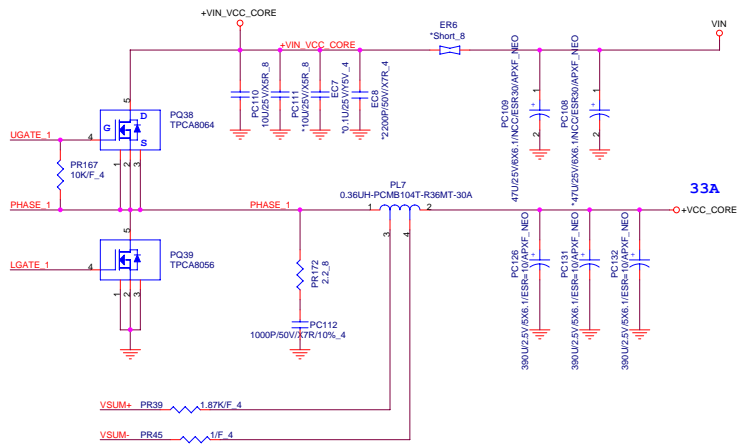
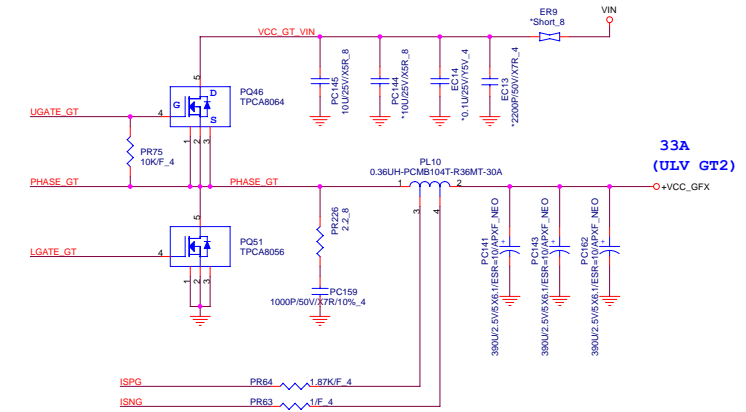
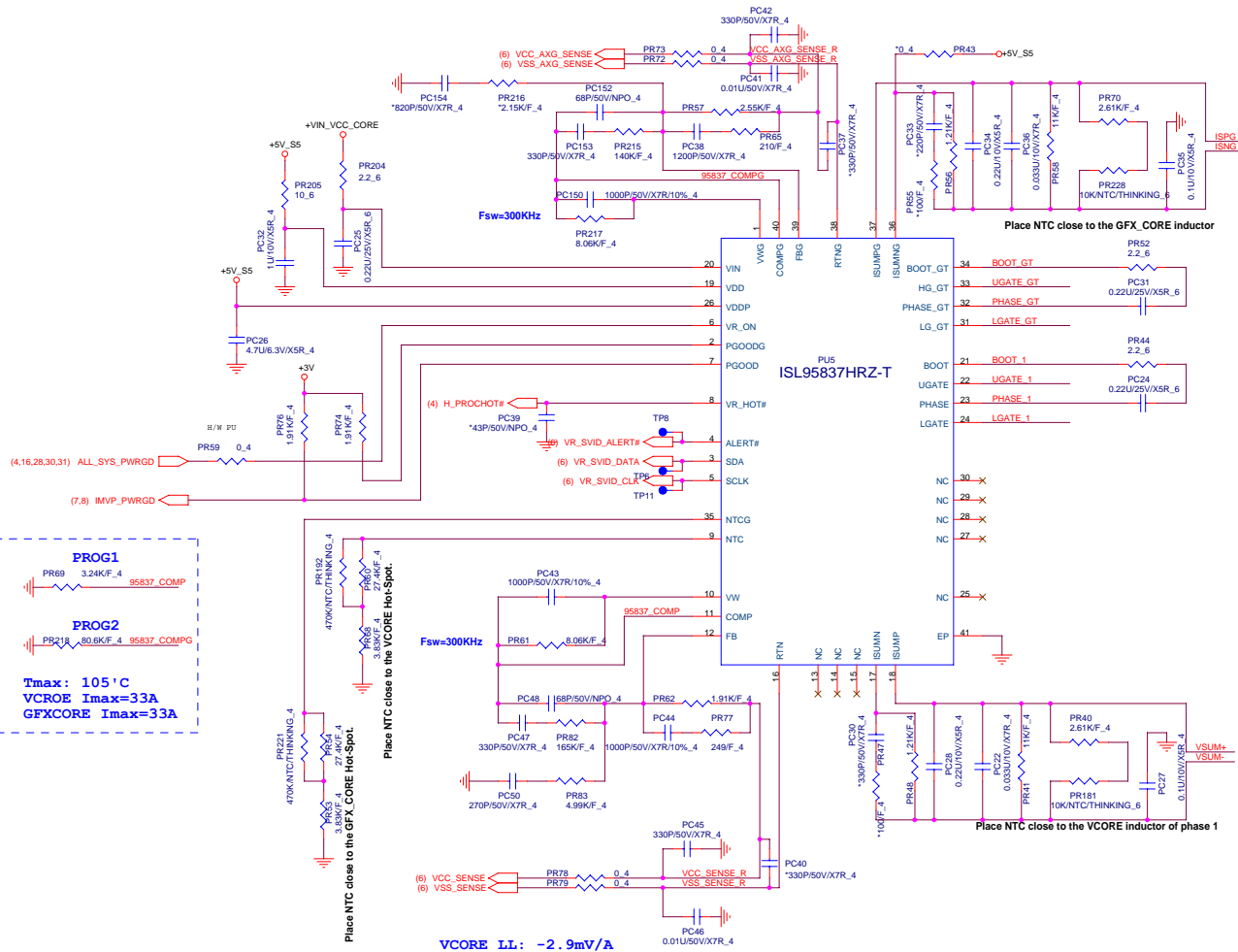


## Power SW Board Connector

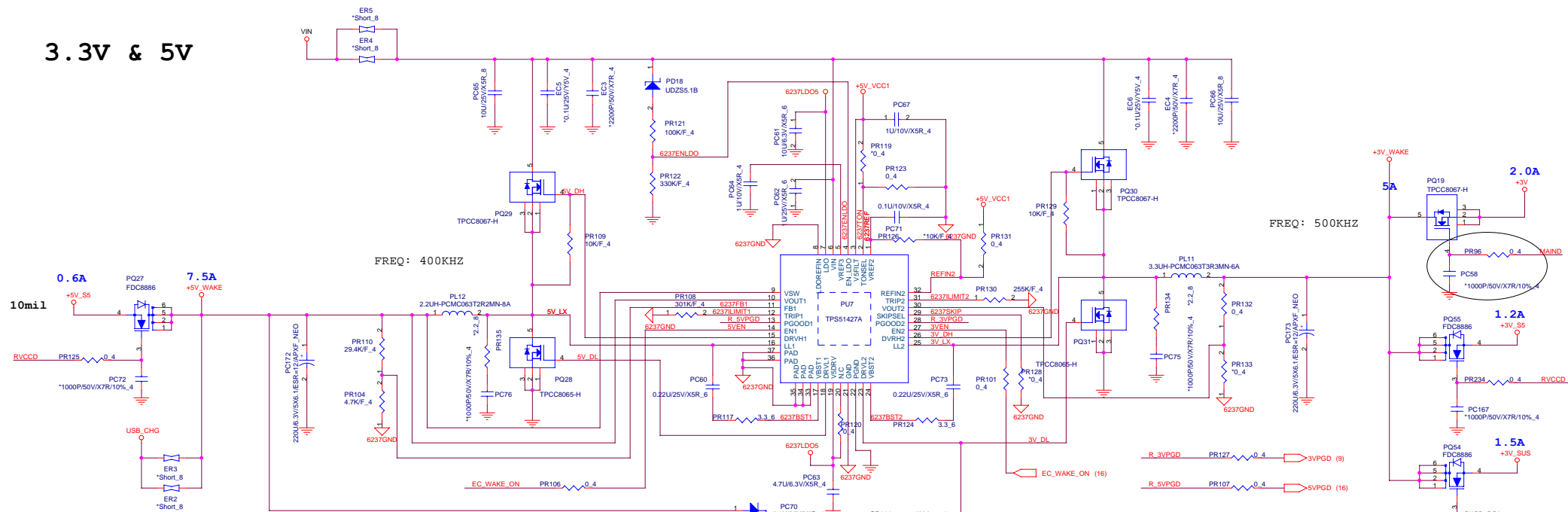


1.Level 1 Environment-related Substances Should Never be Used.	
2.Recycled Resin and Coated Wire should be procured from Green Partners.	2

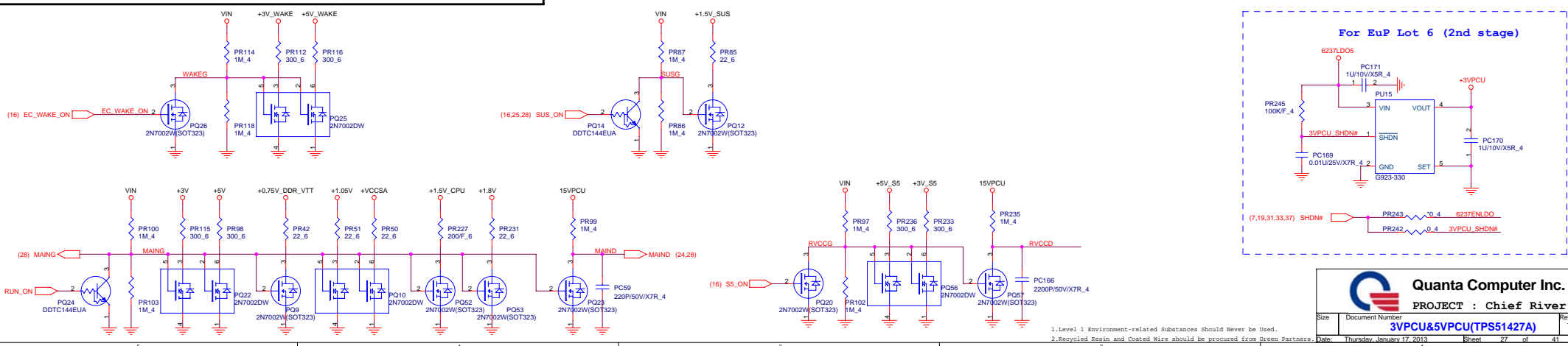
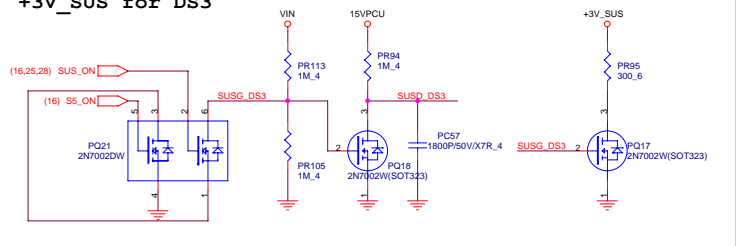
GFX\_CORE LL: -3.9mV/A for GT2



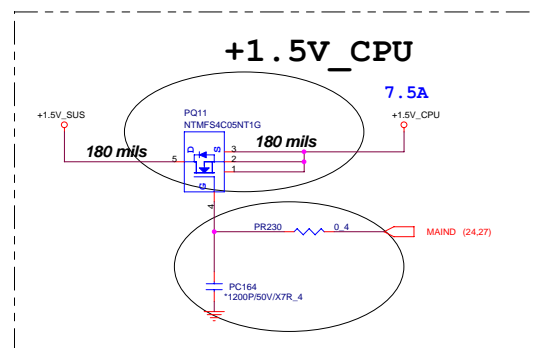
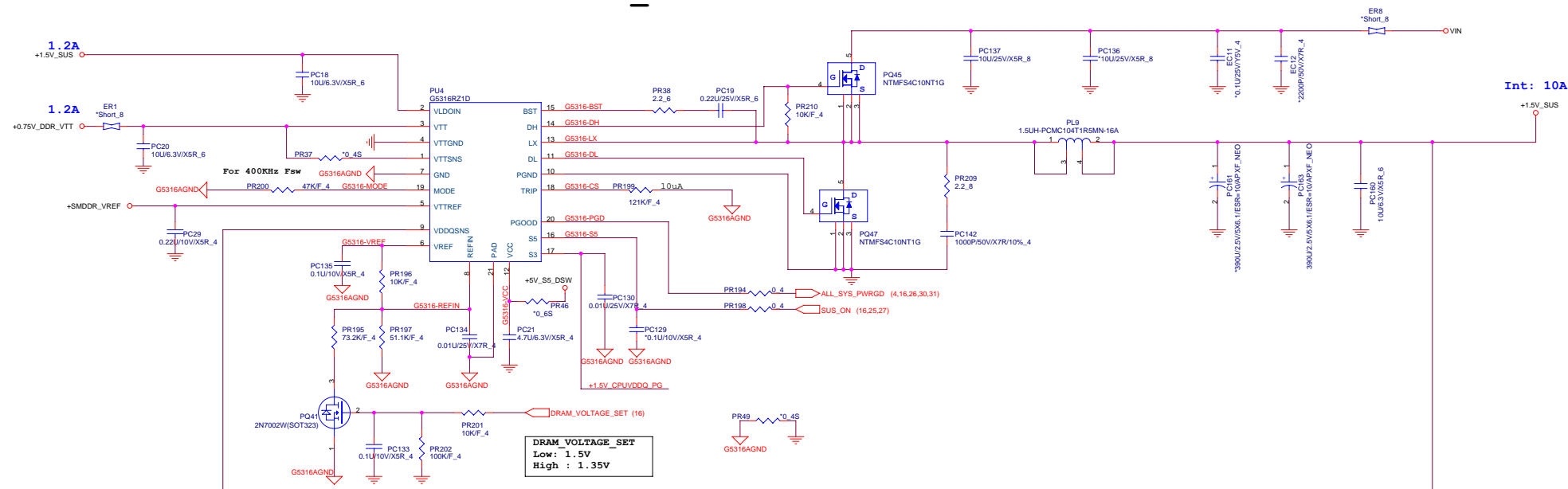
### 3.3V & 5V



## +3V SUS for DS3

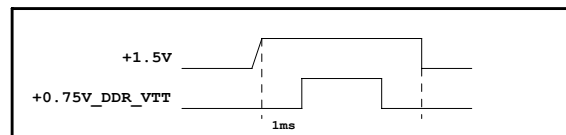
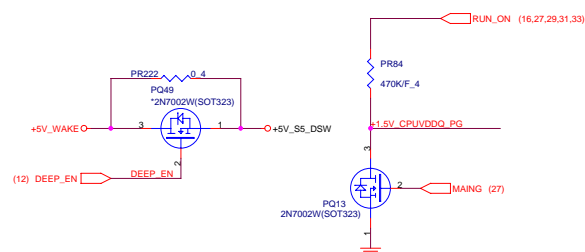


## 1.5VSUS & VTT MEM

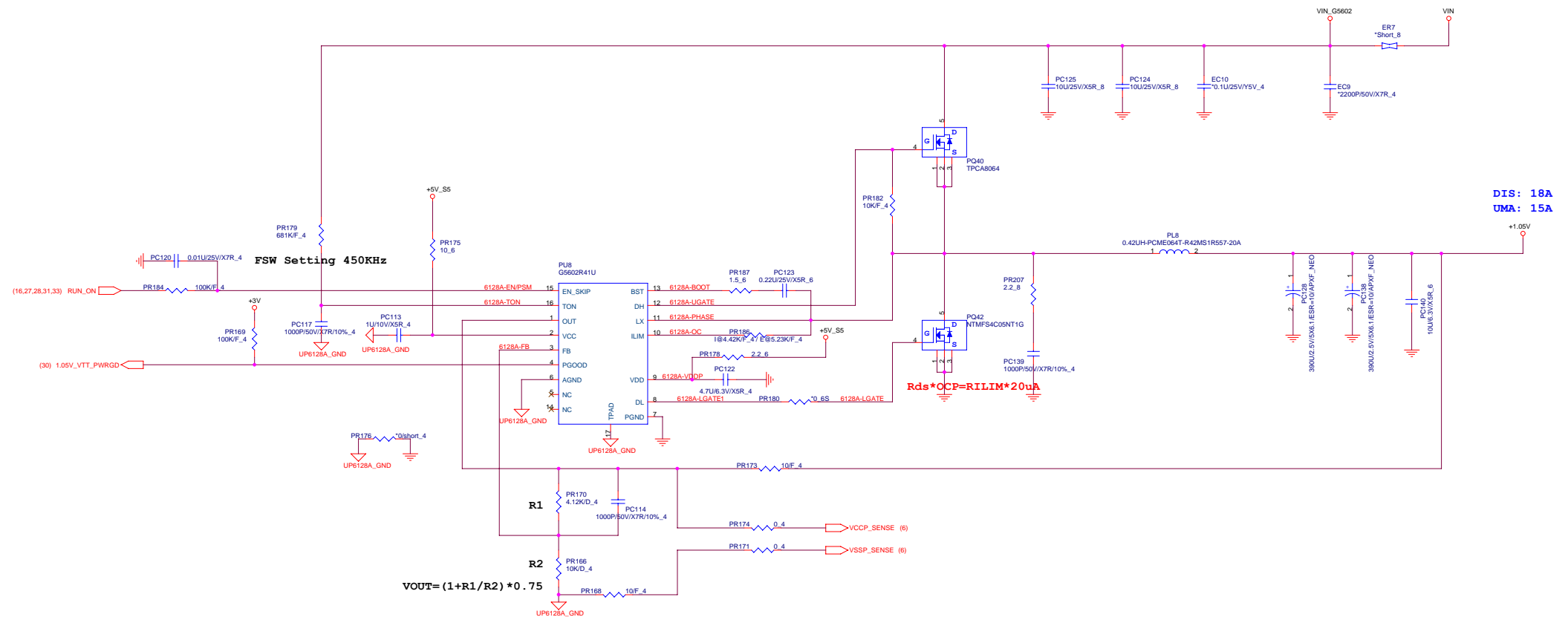


MODE	Resistor on Mode	Fsw	Discharge Mode
3	200Kohm	400KHz	Tracking discharge
2	100Kohm	300KHz	
1	68Kohm	300KHz	Non-tracking discharge
0	47Kohm	400KHz	

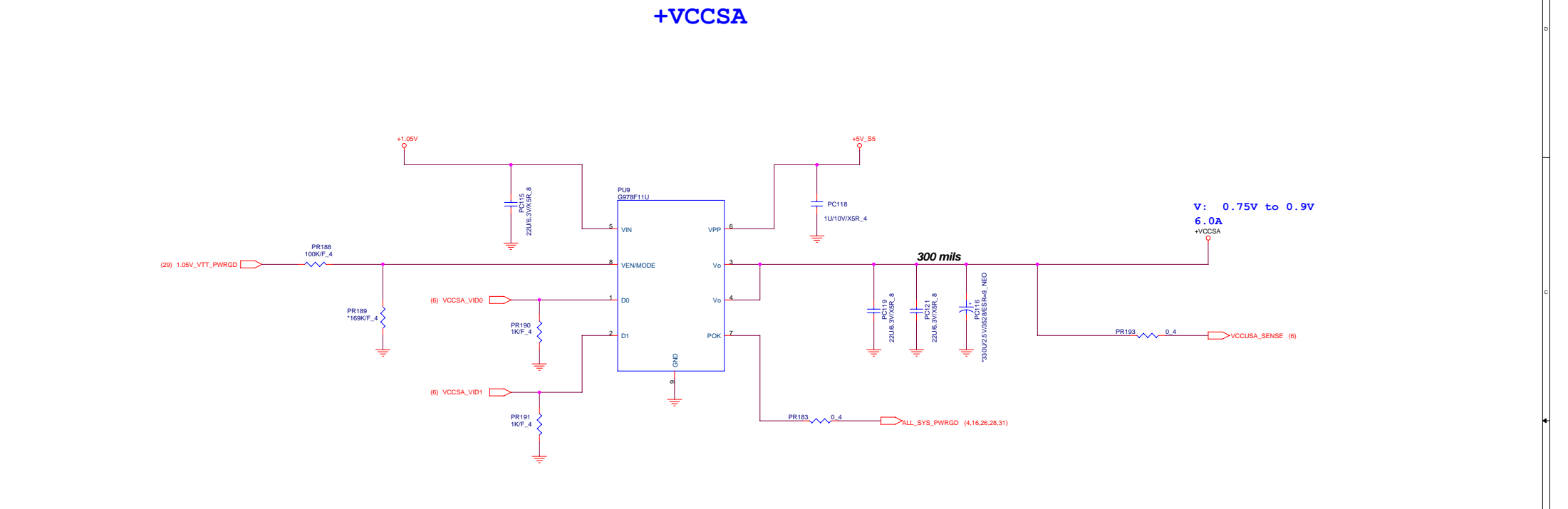
STATE	S3	S5	1.5VSUS	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	Off/High Z
S4/S5	0	0	Off	Off	Off



+1.05V / 15.0A





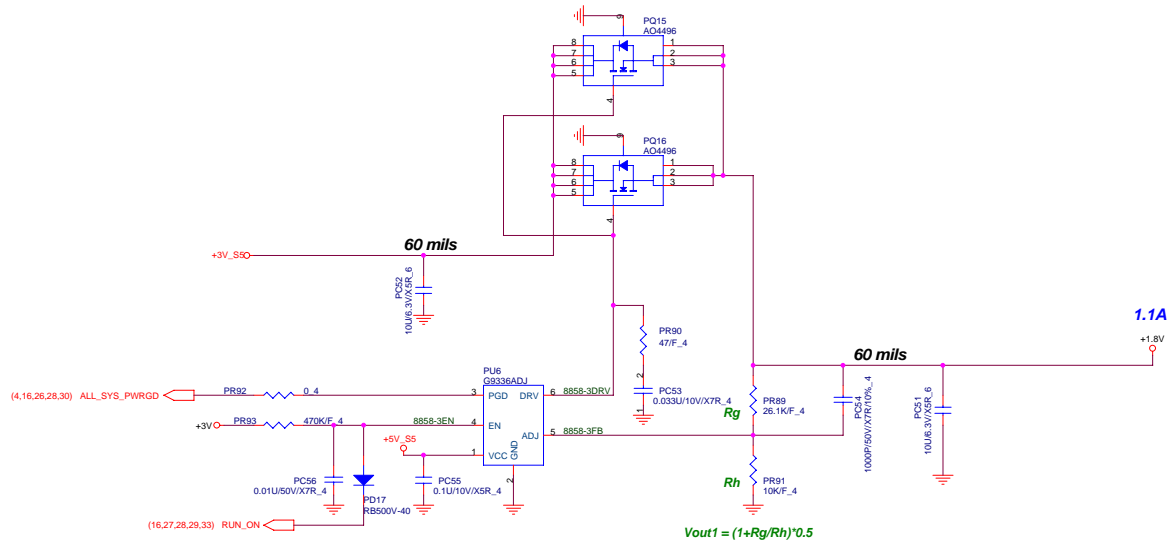


For Chief River ULV

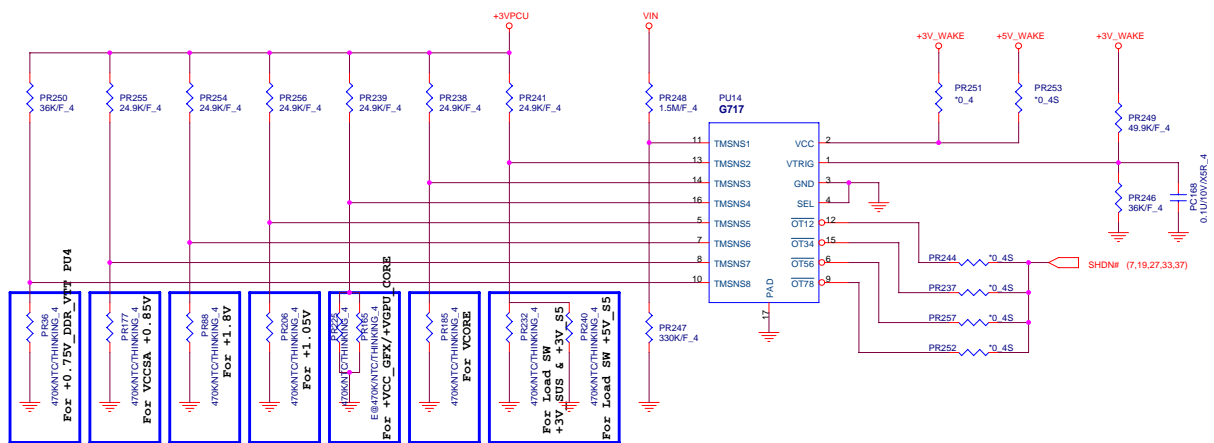
VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

1.Level 1 Environment-related Substances Should Never be Used.  
2.Recycled Resin and Coated Wire should be procured from Green Partners.

## VCC1.8



## Thermal Protection and Battery UVP for VEDS



Quanta Computer Inc.  
PROJECT : Chief River

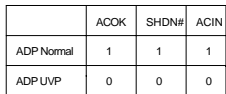
Size	Document Number	Rev
	VCC1.8	1A

1. Level 1 Environment-related Substances Should Never be Used.

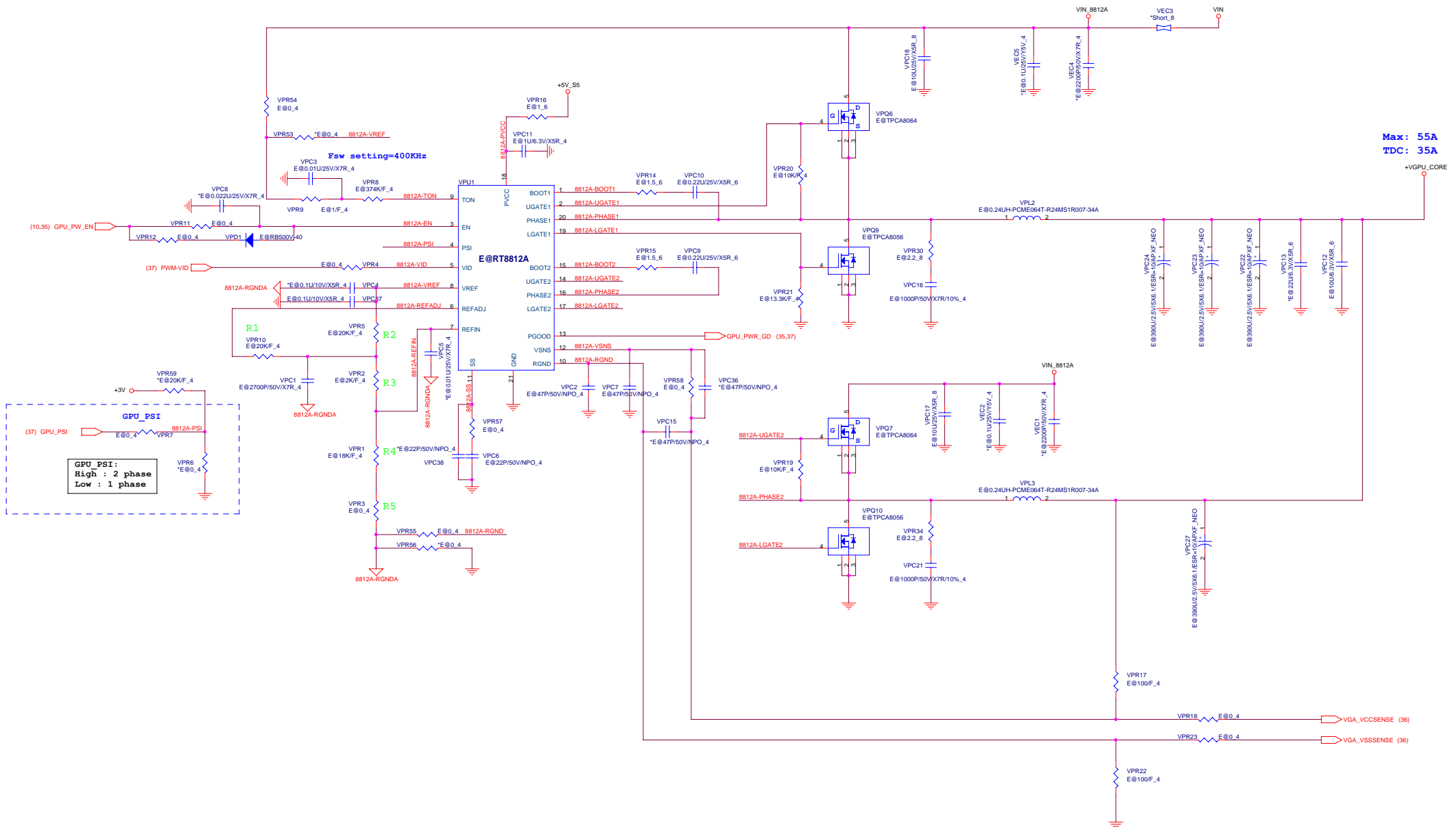
2. Recycled Resin and Coated Wire should be procured from Green Partners.

Date: Thursday, January 17, 2013 Sheet 31 of 41





## VGA-CORE



Quanta Computer Inc.  
PROJECT : Chief River

Size	Document Number	Rev
	VGA_CORE (RT8812A)	1A

1. Level 1 Environment-related Substances Should Never be Used.

2. Recycled Resin and Coated Wire should be procured from Green Partners.

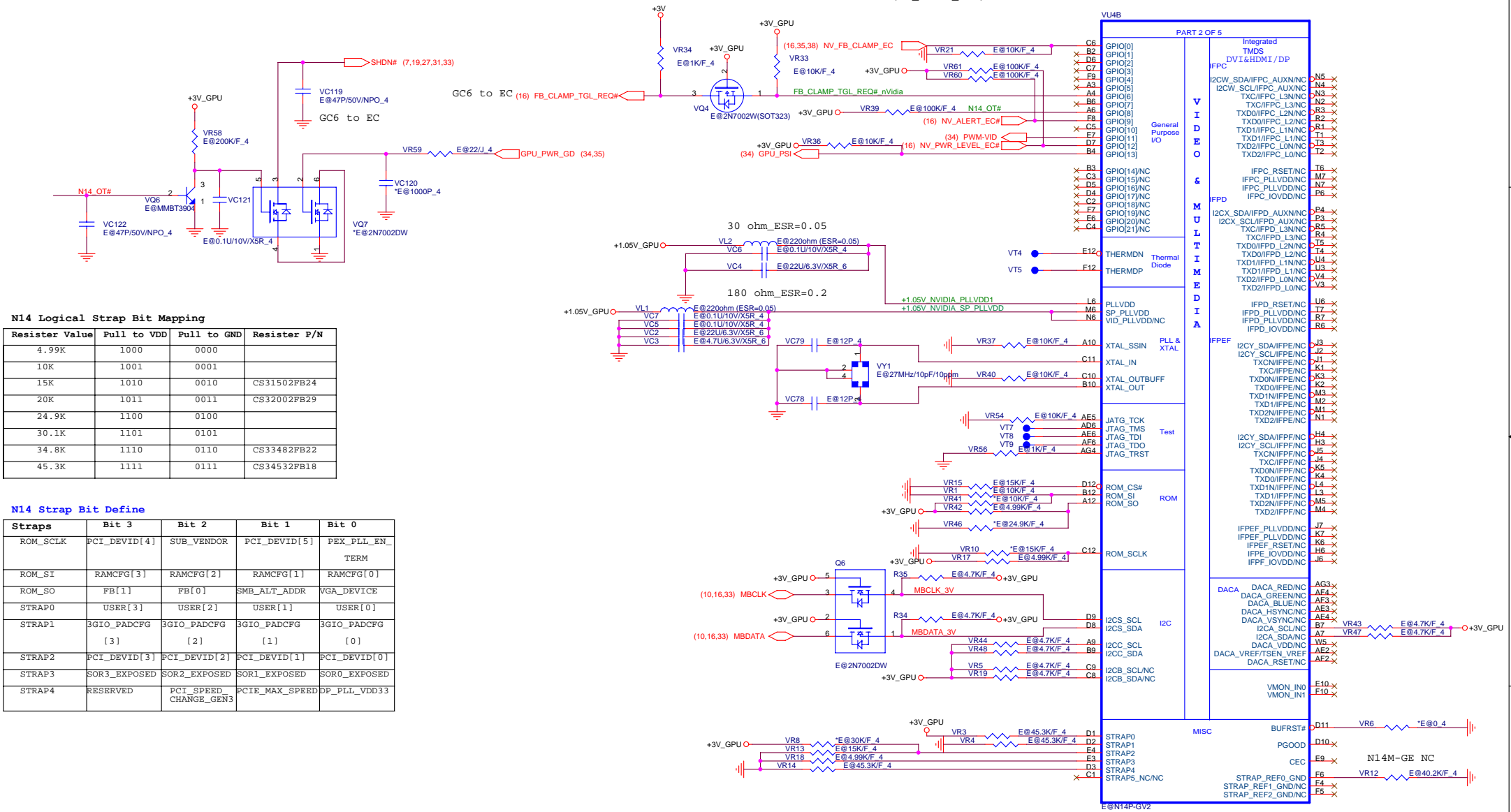
Date: Thursday, January 17, 2013 Sheet: 34 of 41







For GC6 GPU Monitor  
Status(FB\_CLAMP\_MON)

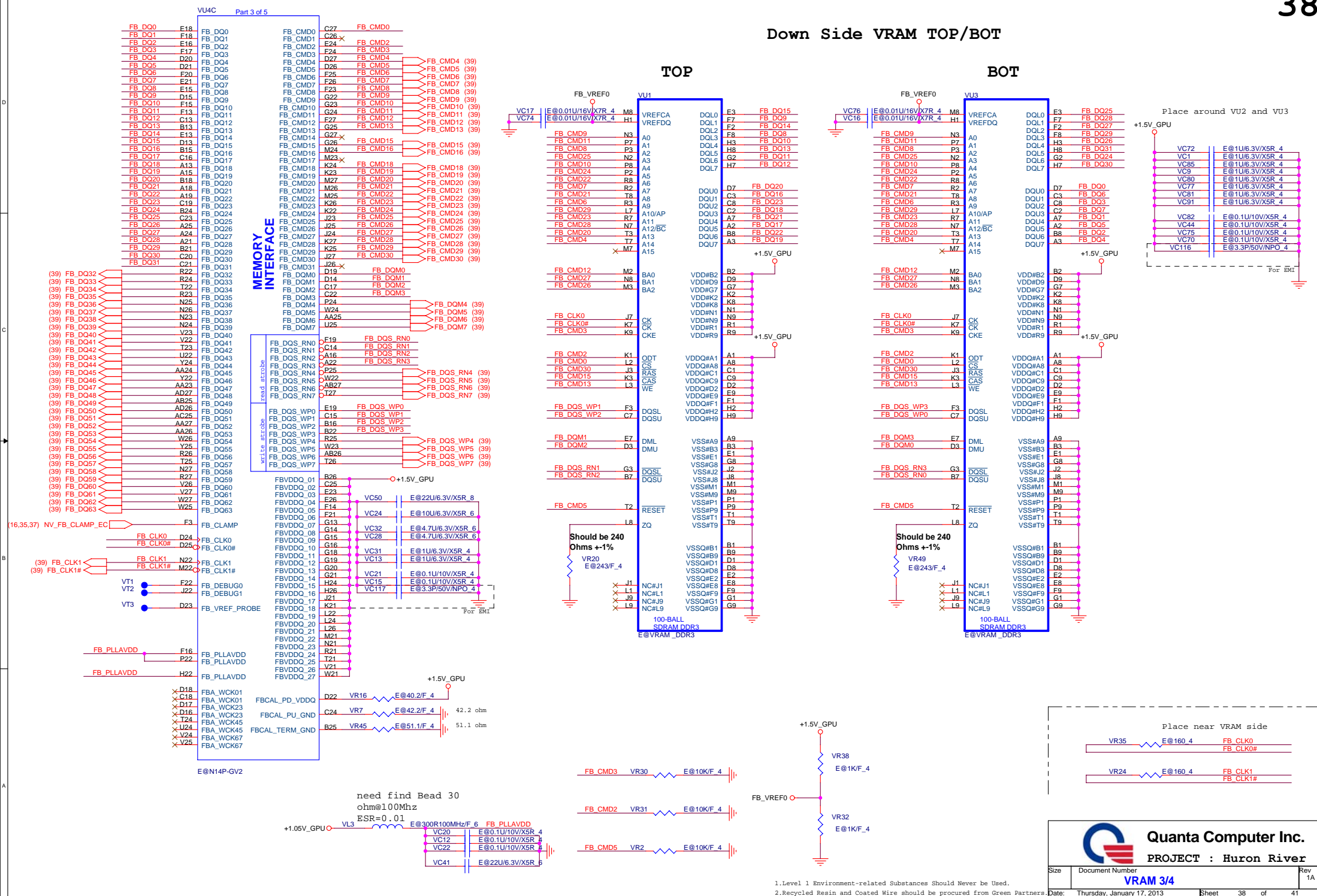


	VRAM Capacity	VRAM Vender	ID	VR1	Mfr P/N	Quanta P/N
N14M-LP N14P-GV2	128Mx16 DDR3	Samsung	0111	PD45.3K	K4W2G1646E-BC11	AKD5MGGT525
		Hynix	0110	PD34.8K	H5TQ2G63DPR-11C	AKD5MGWTW15
	256Mx16 DDR3	Samsung	0011	PD20K	K4W4G1646B-HC11	AKD5MGWT525
		Hynix	0010(TBD)	PD15K	H5TC4G63APR-11C	AKD5PGWTW10

1.Level 1 Environment-related Substances Should Never be Used.  
2.Recycled Resin and Coated Wire should be procured from Green Partners.

<b>Quanta Computer Inc.</b> <b>PROJECT : Huron River</b>		Size	Document Number	Rev 1A
		<b>Nvidia 2/4</b>		
Date:	Thursday, January 17, 2013	Sheet	37	of 41

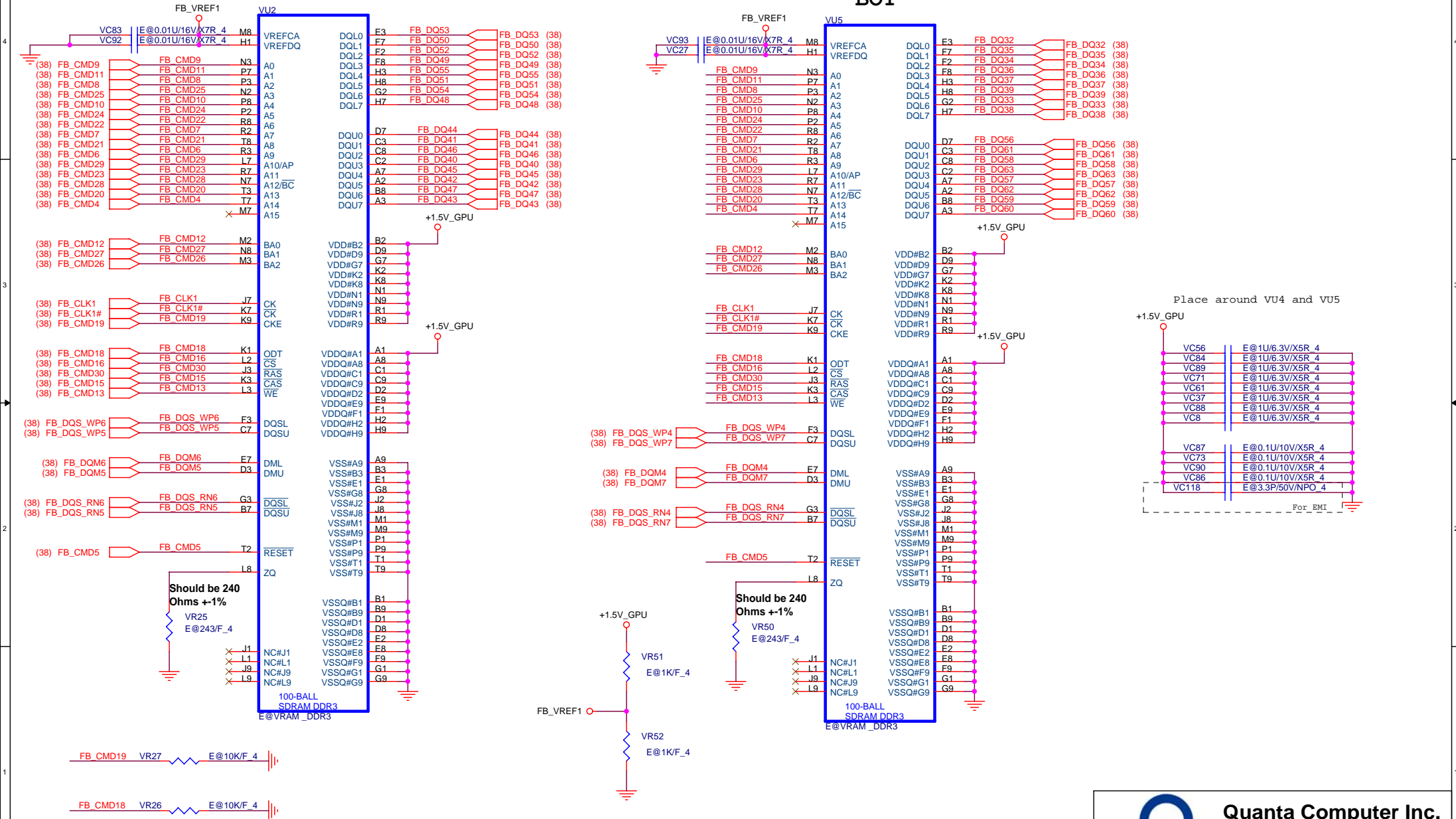
## Down Side VRAM TOP/BOT



## Up Side VRAM TOP/BOT

TOP

BOT



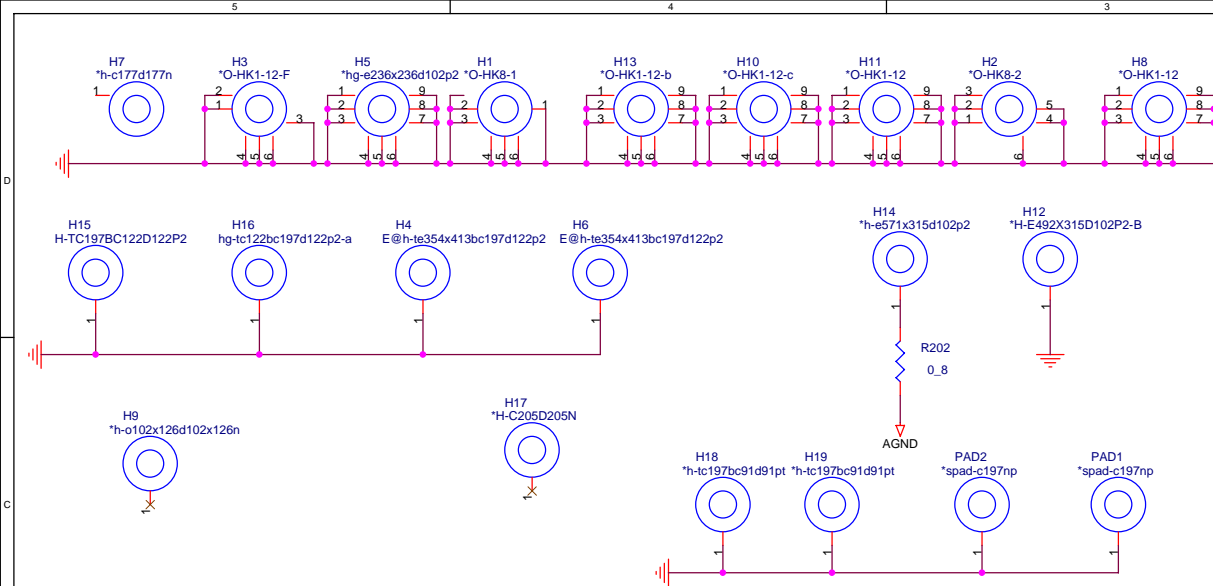
Quanta Computer Inc.

PROJECT : Huron River

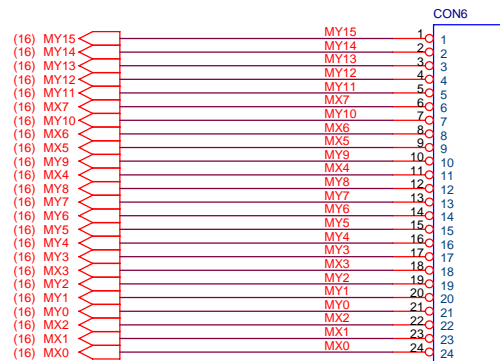
Size	Document Number	Rev
	VRAM 4/4	1A
Date:	Thursday, January 17, 2013	Sheet 39 of 41

1.Level 1 Environment-related Substances Should Never be Used.

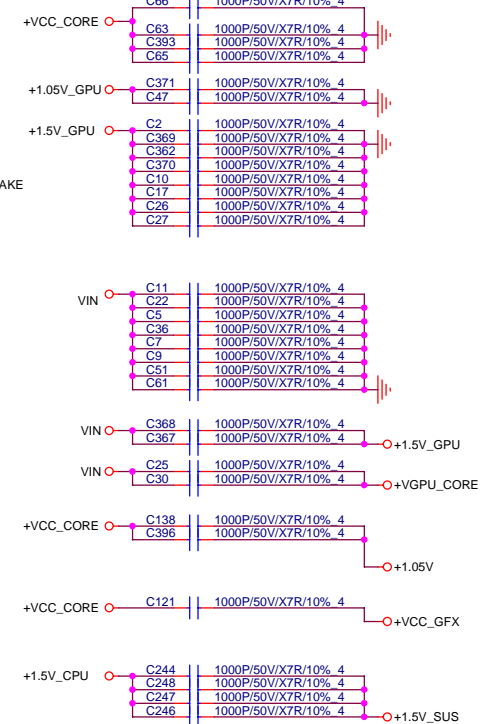
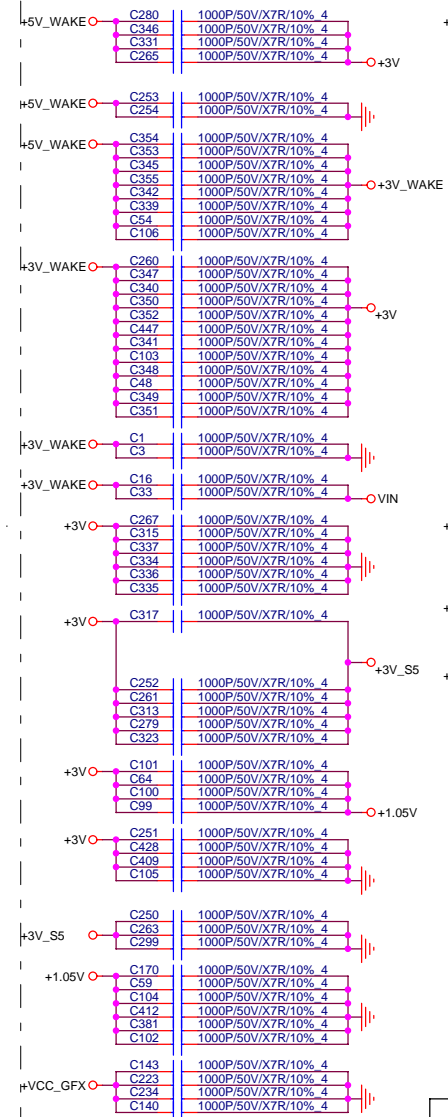
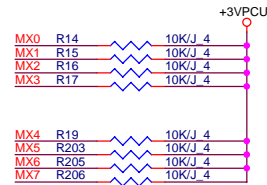
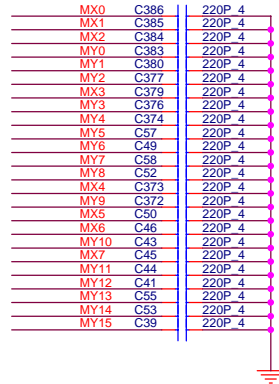
2.Recycled Resin and Coated Wire should be procured from Green Partners.




## KEY BOARD Connector



KB(50503-02441-001)



1. Level 1 Environment-related Substances Should Never be Used.
2. Recycled Resin and Coated Wire should be procured from Green Partners.

 <b>Quanta Computer Inc.</b> PROJECT : HK5		Size	Document Number	Rev	
				1A	
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USB PORT Architecture	
PORT 0	USB3.0
PORT 1	USN3.0
PORT 2	USN2.0
PORT 3	USB2.0
PORT 4	NFC
PORT 5	N/A
PORT 6	N/A
PORT 7	N/A
PORT 8	N/A
PORT 9	WiMax/BT
PORT 10	Camera
PORT 11	Card Reader
PORT 12	Touch Screen
PORT 13	N/A

PCIE BUS	
PORT 1	WLAN Port
PORT 2	CARD READER
PORT 3	GLAN(RTL8111G)
PORT 4	N/A
PORT 5	N/A
PORT 6	N/A
PORT 7	N/A
PORT 8	N/A

SATA BUS	
PORT 0	HDD
PORT 1	N/A
PORT 2	N/A
PORT 3	N/A
PORT 4	ODD
PORT 5	N/A

SM BUS	MBCLK/MBDATA	WRITE	READ	Function
ISL88731CHRTZ	0001 001X	0001 0010	0001 0011	Charger
Nvidia	1001 1110	-	1001 1110	Graphice
LIS331DL	0011 101X	0011 1010	0011 1011	G Sensor

SM BUS	MBCLK_BAT/MBDATA_BAT	WRITE	READ	Function
VGP-BPS35A	0001 011X	0001 0110	0001 0111	Battery

SM BUS	SMB_PCH_CLK/SMB_PCH_DAT	WRITE	READ	Function
DIMM Module0	1010 000X	1010 0000	1010 0001	DDRIII
DIMM Module 1	1010 010X	1010 0100	1010 0101	DDRIII
Synaptics	0010 110X	0010 1100	0010 1101	Click PAD

	0	1
Board ID0	CaspiCRA1-CaspiCRB1 HK8-HK9	SuperiorCRA1-SuperiorCRB1 GD5-GD6
Board ID1	HK8/GD5 14"	HK9/GD6 15"

PCBA SKU	Discrete	UMA
R280(Pull High)	Stuff	No Stuff
R279(Pull Low)	No Stuff	Stuff

	S0	S3	DS3	S4	S5 (Charger Enable)	S5 (Charger Disable)	S5 (Soft OFF) (WoL Disable)	S5 (Soft OFF) (WoL Enable)
RUN_ON	H	L	L	L	L	L	L	L
+3V	H	L	L	L	L	L	L	L
+5V	H	L	L	L	L	L	L	L
+0.75V_DDR_VTT	H	L	L	L	L	L	L	L
+1.05V	H	L	L	L	L	L	L	L
+0.85V	H	L	L	L	L	L	L	L
+1.5V	H	L	L	L	L	L	L	L
+1.8V	H	L	L	L	L	L	L	L
+1.8V_GPU	H	L	L	L	L	L	L	L
+1.0V_GPU	H	L	L	L	L	L	L	L
+VGPU_CORE	H	L	L	L	L	L	L	L
+VCC_GFX	H	L	L	L	L	L	L	L
+VCC_CORE	H	L	L	L	L	L	L	L
SUS_ON	H	H	H	L	L	L	L	L
+1.5V_SUS	H	H	H	L	L	L	L	L
S5_ON	H	H	L	H	L	L	L	H
+5V_S5	H	H	L	H	L	L	L	H
+3V_S5	H	H	L	H	L	L	L	H
EC_WAKE_ON	H	H	H	H	H	L	L	H
+3V_WAKE	H	H	H	H	H	L	L	H
+5V_WAKE	H	H	H	H	H	L	L	H
DEEP_EC_EN	H	H	H	H	L	L	L	L
+3V_S5_DSW	H	H	H	H	L	L	L	L
+3V_SUS	H	H	L	L	L	L	L	L